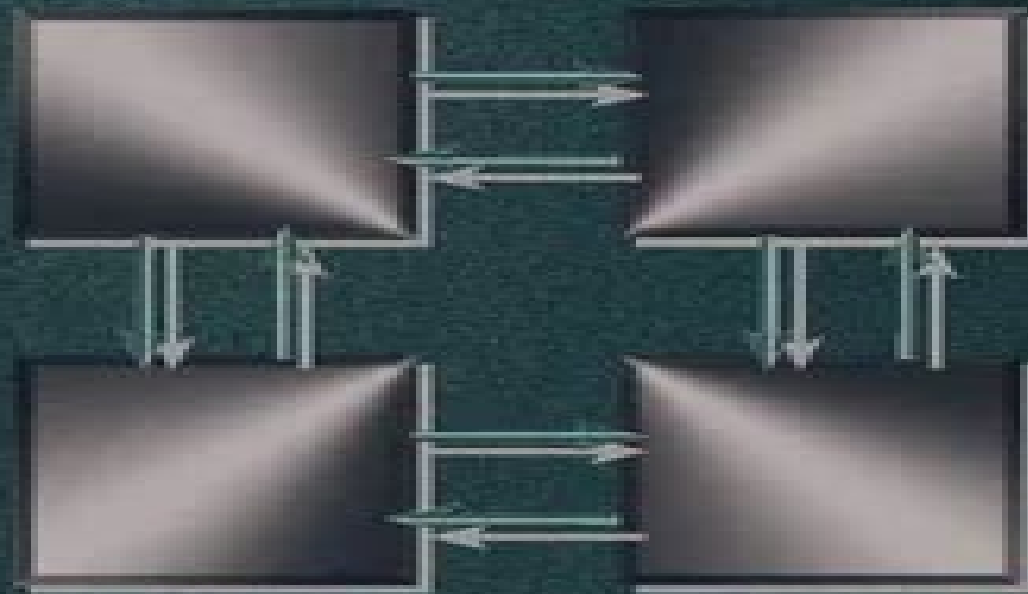


# Specification and Verification of Systolic Arrays



Nam Ling & Magdy A Bayoumi

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# Specification And Verification Of Systolic Arrays

**Shahram Latifi**



## **Specification And Verification Of Systolic Arrays:**

Specification And Verification Of Systolic Arrays Magdy A Bayoumi, Nam Ling, 1999-08-05 Circuits and architectures have become more complex in terms of structure interconnection topology and data flow Design correctness has become increasingly significant as errors in design may result in strenuous debugging or even in the repetition of a costly manufacturing process Although circuit simulation has been used traditionally and widely as the technique for checking hardware and architectural designs it does not guarantee the conformity of designs to specifications Formal methods therefore become vital in guaranteeing the correctness of designs and have thus received a significant amount of attention in the CAD industry today This book presents a formal method for specifying and verifying the correctness of systolic array designs Such architectures are commonly found in the form of accelerators for digital signal image and video processing These arrays can be quite complicated in topology and data flow In the book a formalism called STA is defined for these kinds of dynamic environments with a survey of related techniques A framework for specification and verification is established Formal verification techniques to check the correctness of the systolic networks with respect to the algorithmic level specifications are explained The book also presents a Prolog based formal design verifier named VSTA developed to automate the verification process as using a general purpose theorem prover is usually extremely time consuming Several application examples are included in the book to illustrate how formal techniques and the verifier can be used to automate proofs

**Specification and Verification of Systolic Arrays** Nam Ling, Magdy A. Bayoumi, 1999 Circuits and architectures have become more complex in terms of structure interconnection topology and data flow Design correctness has become increasingly significant as errors in design may result in strenuous debugging or even in the repetition of a costly manufacturing process Although circuit simulation has been used traditionally and widely as the technique for checking hardware and architectural designs it does not guarantee the conformity of designs to specifications Formal methods therefore become vital in guaranteeing the correctness of designs and have thus received a significant amount of attention in the CAD industry today This book presents a formal method for specifying and verifying the correctness of systolic array designs Such architectures are commonly found in the form of accelerators for digital signal image and video processing These arrays can be quite complicated in topology and data flow In the book a formalism called STA is defined for these kinds of dynamic environments with a survey of related techniques A framework for specification and verification is established Formal verification techniques to check the correctness of the systolic networks with respect to the algorithmic level specifications are explained The book also presents a Prolog based formal design verifier named VSTA developed to automate the verification process as using a general purpose theorem prover is usually extremely time consuming Several application examples are included in the book to illustrate how formal techniques and the verifier can be used to automate proofs

Proceedings of the 1993 International Conference on Parallel Processing Alok N. Choudhary, P. Bruce Berra, 1993-08-16

This three volume work presents a compendium of current and seminal papers on parallel distributed processing offered at the 22nd International Conference on Parallel Processing held August 16 20 1993 in Chicago Illinois Topics include processor architectures mapping algorithms to parallel systems performance evaluations fault diagnosis recovery and tolerance cube networks portable software synchronization compilers hypercube computing and image processing and graphics Computer professionals in parallel processing distributed systems and software engineering will find this book essential to their complete computer reference library Algorithm Engineering for Integral and Dynamic Problems Lucia

Rapanotti,2001-01-23 Algorithm engineering allows computer engineers to produce a computational machine that will execute an algorithm as efficiently and cost effectively as possible given a set of constraints such as minimal performance or the availability of technology Addressing algorithm engineering in a parallel setting regular array syntheses offer powerful computation and embody best practice but often face the criticism that they are applicable only to restricted classes of algorithms Algorithm Engineering for Integral and Dynamic Problems reviews the basic principles of regular array synthesis and shows how to extend its use into classes of algorithms traditionally viewed to be beyond its domain of application The author discusses the transformation of the initial algorithm specification into a specification with data dependencies of increased regularity in order to obtain corresponding regular arrays by direct application of the standard mapping techniques The book includes a review of the basic principles of regular array synthesis followed by applications of these techniques to well known algorithms concluding with numerous case studies to illustrate the methods Researchers and practitioners in algorithm engineering will find that this text significantly extends their understanding of the applications of regular array synthesis and regular array processors beyond the traditionally narrow field of relevance **PARLE '92,**

**Parallel Architectures and Languages Europe** Daniel Etiemble,1992-06-03 The 1992 Parallel Architectures and Languages Europe conference continues the tradition of a wide and representative international meeting of specialists from academia and industry in theory design and application of parallel computer systems set by the previous PARLE conferences held in Eindhoven in 1987 1989 and 1991 This volume contains the 52 regular and 25 poster papers that were selected from 187 submitted papers for presentation and publication In addition five invited lectures are included The regular papers are organized into sections on implementation of parallel programs graph theory architecture optimal algorithms graph theory and performance parallel software components data base optimization and modeling data parallelism formal methods systolic approach functional programming fine grain parallelism Prolog data flow systems network efficiency parallel algorithms cache systems implementation of parallel languages parallel scheduling in data base systems semantic models parallel data base machines and language semantics **ITNG 2023 20th International Conference on Information**

**Technology-New Generations** Shahram Latifi,2023-05-06 This volume represents the 20th International Conference on Information Technology New Generations ITNG 2023 ITNG is an annual event focusing on state of the art technologies

pertaining to digital information and communications The applications of advanced information technology to such domains as astronomy biology education geosciences security and health care are the among topics of relevance to ITNG Visionary ideas theoretical and experimental results as well as prototypes designs and tools that help the information readily flow to the user are of special interest Machine Learning Robotics High Performance Computing and Innovative Methods of Computing are examples of related topics The conference features keynote speakers a best student award poster award service award a technical open panel and workshops exhibits from industry government and academia This publication is unique as it captures modern trends in IT with a balance of theoretical and experimental work Most other work focus either on theoretical or experimental but not both Accordingly we do not know of any competitive literature **Transformational Approaches to Systolic Design** G. M. Megson,1994 Computer Systems Organization Processor Architectures Architecture of High Performance Computers Volume II R. IBETT,2013-11-11 A Systolic Array Optimizing Compiler Monica S. Lam,2012-12-06 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high performance programmable systolic arrays represents a practical cost effective solution to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors *Вычислительные Машины И Искусственный Интеллект* ,1993 Computer Hardware Description Languages and their Applications D. Agnew,L. Claesen,R. Camposano,2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal

reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification     Theoretical Foundations of VLSI Design K. McEvoy,J. V. Tucker,2003-12-04 Recent research on the physical technologies of very large scale integration VLSI     Logic and Algebra of Specification Friedrich L. Bauer,Wilfried Brauer,Helmut Schwichtenberg,2012-12-06 For some years specification of software and hardware systems has been influenced not only by algebraic methods but also by new developments in logic These new developments in logic are partly based on the use of algorithmic techniques in deduction and proving methods but are alsodue to new theoretical advances to a great extent stimulated by computer science which have led to new types of logic and new logical calculi The new techniques methods and tools from logic combined with algebra based ones offer very powerful and useful tools for the computer scientist which may soon become practical for commercial use where in particular more powerful specification tools are needed for concurrent and distributed systems This volume contains papers based on lectures by leading researchers which were originally given at an international summer school held in Marktoberdorf in 1991 The papers aim to give a foundation for combining logic and algebra for the purposes of specification under the aspects of automated deduction proving techniques concurrency and logic abstract data types and operational semantics and constructive methods     Proceedings of the 31st Midwest Symposium on Circuits and Systems, August 9-12, 1988, Marriott's Pavilion Hotel, St. Louis, Missouri Linda R. Laub,R. Eugene Stuffle,University of Missouri--Rolla. Engineering Continuing Education,University of Missouri--Rolla. Dept. of Electrical Engineering,1988     *Proceedings of the International Conference on Application Specific Array Processors, September 2-4, 1991, Barcelona, Spain* Mateo Valero,1991 The International Conference on Application Specific Array Processors ASAP 91 was held September 1991 in Barcelona Spain Application specific computing may be the solution to many computationally intensive problems Coverage here includes design mapping techniques synthesis and verification and systolic array designs and design methodologies No index Annotation copyrighted by Book News Inc Portland OR

**Proceedings of the ... Midwest Symposium on Circuits and Systems** ,1993     *Theorem Provers in Circuit Design* Ramayya Kumar,Thomas Kropf,1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering     **Formal Hardware Verification** Thomas Kropf,1997-08-27 This state of the art monograph presents a coherent survey of a variety of methods and systems for formal hardware verification It emphasizes the presentation of approaches that have matured into tools and systems usable for the actual

verification of nontrivial circuits All in all the book is a representative and well structured survey on the success and future potential of formal methods in proving the correctness of circuits The various chapters describe the respective approaches supplying theoretical foundations as well as taking into account the application viewpoint By applying all methods and systems presented to the same set of IFIP WG10.5 hardware verification examples a valuable and fair analysis of the strengths and weaknesses of the various approaches is given *Scientific and Technical Aerospace Reports*, 1989

**Logic, Algebra, and Computation** Friedrich L. Bauer, 2012-12-06 The Marktoberdorf Summer Schools on Informatics were started in 1970 with the intention to convene every second or third year a group of top researchers in computing devoted to preach their most recent results to an elite of advanced students young and most promising people and prepared to stand their questions criticism and suggestions The themes of these Advanced Study Institutes under the sponsorship of the NATO Scientific Affairs Division varied slightly over the years oscillating more or less around Programming Methodology as the following list shows 1970 Data Structures and Computer Systems 1971 Program Structures and Fundamental Concepts of Programming 1973 Structured Programming and Programmed Structures 1975 Language Hierarchies and Interfaces 1978 Program Construction 1981 Theoretical Foundations of Programming Methodology 1984 Control Flow and Data Flow Concepts of Distributed Programming 1986 Logic of Programming and Calculi of Discrete Design 1988 Constructive Methods in Computing Science 1989 Logic Algebra and Computation Logic Algebra and Computation is the theme of the summer school to which this volume is devoted It is the tenth in succession but it is also the first in a new series the blue series that is intended to alternate in future with the traditional the red series arrangement in fact the tenth summer school in the red series with the title Programming and Mathematical Method held in 1990 was the subject of celebrating both its serial number and the twenty years of Marktoberdorf Summer Schools altogether

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