

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

**Edited by
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Soc Systemonachip Testing For Plug And Play Test Automation

Wolfgang Maichen



Soc Systemonachip Testing For Plug And Play Test Automation:

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2002-09-30 Various aspects of system on a chip SOC integrated circuit testing are addressed in 13 papers on test planning access and scheduling test data compression and interconnect crosstalk and signal integrity Topics include concurrent test of core based SOC design and testing for interconnect crosstalk defects using on chip embedded processor cores The editor is affiliated with Duke University The book is reprinted from a Special Issue of the Journal of Electronic Testing vol 18 nos 4 5 There is no subject index Annotation c 2003 Book News Inc Portland OR booknews com *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation* Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing *Soc (System-On-a-Chip) Testing for Plug and Play Test Automation* Springer, 2014-01-15 **Introduction to Advanced System-on-Chip Test Design and Optimization** Erik Larsson, 2006-03-30 SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process *Test Resource Partitioning for System-on-a-Chip* Vikram Iyengar, Anshuman Chandra, 2012-12-06 Test Resource Partitioning for System on a Chip is about test resource partitioning and optimization techniques for plug and play system on a chip SOC test automation Plug and play refers to the paradigm in which core to core interfaces as well as core to SOC logic interfaces are standardized such that cores can be easily plugged into virtual sockets on the SOC design and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator The goal of the book is to position test resource partitioning in the context of SOC test automation as well as to generate interest and

motivate research on this important topic SOC integrated circuits composed of embedded cores are now commonplace Nevertheless There remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols Test Resource Partitioning for System on a Chip responds to a pressing need for a structured methodology for SOC test automation It presents new techniques for the partitioning and optimization of the three major SOC test resources test hardware testing time and test data volume Test Resource Partitioning for System on a Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug and play fashion The framework presented allows the system integrator to reduce test cost and meet short time to market requirements

Reliability, Availability and Serviceability of Networks-on-Chip Érika Cota,Alexandre de Moraes Amory,Marcelo Soares Lubaszewski,2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures

Advances in Electronic Testing Dimitris Gizopoulos,2006-01-22 Advances in Electronic Testing Challenges and Methodologies is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing The book is a comprehensive elaboration on important topics which capture major research and development efforts today The motivation and inspiration behind this book is to deliver a thorough text that focuses on the evolution of test technology provides insight about the abiding importance of discussed topics records today s state of the art and industrial practices and trends reveals the challenges for emerging testing methodologies and envisages the future of this journey The book consists of eleven edited chapters written by experts in Defect Oriented Testing Nanometer Technologies Failures and Testing Silicon Debug Delay Testing High Speed Test Interfaces DFT Oriented Low Cost Testers Embedded Cores and System on Chip Testing Memory Testing Mixed Signal Testing RF Testing and Loaded Board Testing Contributing authors are affiliated with in alphabetical order Agilent ARM Balearic Islands Univ IBM Inovys Intel LogicVision Magma Mentor Graphics New Mexico Univ Sandia National Labs Synopsys Teradyne and Texas Instruments Advances in Electronic Testing Challenges and Methodologies is an advanced textbook and reference point for senior undergraduate and graduate students in MSc or PhD tracks professors and research leaders in the electronic testing domain It is also for industry design and test engineers and managers seeking a global view and understanding of test technology practices and methodologies and a dense elaboration on test related issues they face in their development projects There is a definite need for documenting the advances in testing I find the work of this edited volume by Dimitris Gizopoulos and his team of authors to be significant and timely the

book provides besides novel test methodologies a collective insight into the emerging aspects of testing This I think is beneficial to practicing engineers and researchers both of whom must stay at the forefront of technology This latest addition to the Frontiers Series is destined to serve an important role From the Foreword by Vishwani D Agrawal Consulting Editor Frontiers in Electronic Testing Book Series Oscillation-Based Test in Mixed-Signal Circuits Gloria Huertas Sánchez, Diego Vázquez García de la Vega, Adoración Rueda Rueda, Jose Luis Huertas Díaz, 2007-06-03 Oscillation Based Test in Mixed Signal Circuits presents the development and experimental validation of the structural test strategy called Oscillation Based Test OBT in short The results here presented allow to assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits **The Core Test Wrapper Handbook** Francisco da Silva, Teresa McLaurin, Tom Waayers, 2006-09-15 In the early to mid 1990 s while working at what was then Motorola Semiconductor business changes forced my multi hundred dollar microprocessor to become a tens of dollars embedded core I ran into first hand the problem of trying to deliver what used to be a whole chip with something on the order of over 400 interconnect signals to a design team that was going to stuff it into a package with less than 220 signal pins and surround it with other logic I also ran into the problem of delivering microprocessor specification verification a microprocessor is not just about the functions and instructions included with the instruction set but also the MIPs rating at some given frequency I faced two dilemmas one I could not deliver functional vectors without significant development of off core logic to deal with the reduced chip I/O map and everybody's I/O map was going to be a little different and two the JTAG 1149.1 boundary scan ring that was around my core when it was a chip was going to be woefully inadequate since it did not support speed signal application and capture and independent use separate from my core I considered the problem at length and came up with my own solution that was predominantly a separate non JTAG scan test wrapper that supported at speed application of launch capture cycles using the system clock But my problems weren't over at that point either Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are

applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent

Soc Systemonachip Testing For Plug And Play Test Automation Book Review: Unveiling the Power of Words

In some sort of driven by information and connectivity, the ability of words has be more evident than ever. They have the capability to inspire, provoke, and ignite change. Such could be the essence of the book **Soc Systemonachip Testing For Plug And Play Test Automation**, a literary masterpiece that delves deep in to the significance of words and their affect our lives. Compiled by a renowned author, this captivating work takes readers on a transformative journey, unraveling the secrets and potential behind every word. In this review, we will explore the book is key themes, examine its writing style, and analyze its overall effect on readers.

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