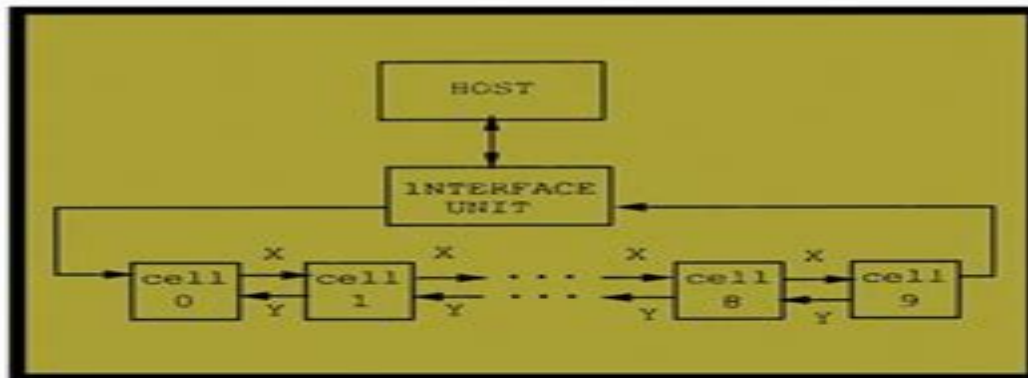

A Systolic Array Parallelizing Compiler

Ping-Sheng Tseng

foreword by H. T. Kung



Kluwer Academic Publishers

Systolic Array Parallelizing Compiler

Ensheng Dong



Systolic Array Parallelizing Compiler:

A Systolic Array Parallelizing Compiler, 1990-08-31 *A Systolic Array Parallelizing Compiler* Ping-Sheng Tseng, 2012-12-06 Widespread use of parallel processing will become a reality only if the process of porting applications to parallel computers can be largely automated Usually it is straightforward for a user to determine how an application can be mapped onto a parallel machine however the actual development of parallel code if done by hand is typically difficult and time consuming Parallelizing compilers which can generate parallel code automatically are therefore a key technology for parallel processing In this book Ping Sheng Tseng describes a parallelizing compiler for systolic arrays called AL Although parallelizing compilers are quite common for shared memory parallel machines the AL compiler is one of the first working parallelizing compilers for distributed memory machines of which systolic arrays are a special case The AL compiler takes advantage of the fine grain and high bandwidth interprocessor communication capabilities in a systolic architecture to generate efficient parallel code xii Foreword While capable of handling an important class of applications AL is not intended to be a general purpose parallelizing compiler *A Systolic Array Optimizing Compiler* Monica S. Lam, 2011-10-17 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high performance programmable systolic arrays represents a practical cost effective solution to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors Parallel Computing and Transputers D. Arnold, 1994 The broadening of interest in parallel computing and transputers is reflected in this text Topics covered include concurrent programming graphics and image processing and robotics and control It is based on the proceedings of the 6th Australian Transputer and Occam User Group *Software for Parallel Computation* Janusz S. Kowalik, Lucio Grandinetti, 2012-12-06 This volume contains papers presented at the NATO sponsored Advanced Research Workshop on Software for Parallel Computation held at the University of Calabria Cosenza

Italy from June 22 to June 26 1992 The purpose of the workshop was to evaluate the current state of the art of the software for parallel computation identify the main factors inhibiting practical applications of parallel computers and suggest possible remedies In particular it focused on parallel software programming tools and practical experience of using parallel computers for solving demanding problems Critical issues relative to the practical use of parallel computing included portability reusability and debugging parallelization of sequential programs construction of parallel algorithms and performance of parallel programs and systems In addition to NATO the principal sponsor the following organizations provided a generous support for the workshop CERFACS France C I R A Italy C N R Italy University of Calabria Italy ALLENIA Italy The Boeing Company U S A CISE Italy ENEL D S R Italy Alliant Computer Systems Bull RN Sud Italy Convex Computer Digital Equipment Corporation Hewlett Packard Meiko Scientific U K PARSYTEC Computer Germany TELMAT Informatique France Thinking Machines Corporation

Automatic Parallelization for a Class of Regular Computations

G. M. Megson, Xian Chen, 1997 The automatic generation of parallel code from high level sequential description is of key importance to the wide spread use of high performance machine architectures This text considers in detail the theory and practical realization of automatic mapping of algorithms generated from systems of uniform recurrence equations do lccps onto fixed size architectures with defined communication primitives Experimental results of the mapping scheme and its implementation are given

Languages and Compilers for Parallel Computing

Charith Mendis, Lawrence Rauchwerger, 2023-05-09 This book constitutes the thoroughly refereed post conference proceedings of the 35th International Workshop on Languages and Compilers for Parallel Computing LCPC 2022 held in Chicago IL USA in October 2022 The 9 revised full papers were carefully reviewed and selected from 12 submissions The conference covers all aspects of languages compiler techniques run time environments and compiler related performance evaluation for parallel and high performance computing The scope of the workshop encompasses foundational results as well as practical experience reports and bold new ideas for future systems

Algorithms for Parallel Processing

Michael T. Heath, Abhram Ranade, Robert S. Schreiber, 2012-12-06 This IMA Volume in Mathematics and its Applications ALGORITHMS FOR PARALLEL PROCESSING is based on the proceedings of a workshop that was an integral part of the 1996 97 IMA program on MATHEMATICS IN HIGH PERFORMANCE COMPUTING The workshop brought together algorithm developers from theory combinatorics and scientific computing The topics ranged over models linear algebra sorting randomization and graph algorithms and their analysis We thank Michael T Heath of University of Illinois at Urbana Computer Science Abhram Ranade of the Indian Institute of Technology Computer Science and Engineering and Robert S Schreiber of Hewlett Packard Laboratories for their excellent work in organizing the workshop and editing the proceedings We also take this opportunity to thank the National Science Foundation NSF and the Army Research Office ARO whose financial support made the workshop possible A vner Friedman Robert Gulliver v

PREFACE The Workshop on Algorithms for Parallel Processing was held at the IMA September

16 20 1996 it was the first workshop of the IMA year dedicated to the mathematics of high performance computing The workshop organizers were Abhiram Ranade of The Indian Institute of Technology Bombay Michael Heath of the University of Illinois and Robert Schreiber of Hewlett Packard Laboratories Our idea was to bring together researchers who do innovative exciting parallel algorithms research on a wide range of topics and by sharing insights problems tools and methods to learn something of value from one another

Compiler Optimizations for Scalable Parallel Systems Santosh Pande, Dharma P. Agrawal, 2003-06-29 Scalable parallel systems or more generally distributed memory systems offer a challenging model of computing and pose fascinating problems regarding compiler optimization ranging from language design to run time systems Research in this area is foundational to many challenges from memory hierarchy optimizations to communication optimization This unique handbook like monograph assesses the state of the art in the area in a systematic and comprehensive way The 21 coherent chapters by leading researchers provide complete and competent coverage of all relevant aspects of compiler optimization for scalable parallel systems The book is divided into five parts on languages analysis communication optimizations code generation and run time systems This book will serve as a landmark source for education information and reference to students practitioners professionals and researchers interested in updating their knowledge about or active in parallel computing

Languages and Compilers for Parallel Computing Chua-Huang Huang, 1996-01-24 This book presents the refereed proceedings of the Eighth Annual Workshop on Languages and Compilers for Parallel Computing held in Columbus Ohio in August 1995 The 38 full revised papers presented were carefully selected for inclusion in the proceedings and reflect the state of the art of research and advanced applications in parallel languages restructuring compilers and runtime systems The papers are organized in sections on fine grain parallelism interprocedural analysis program analysis Fortran 90 and HPF loop parallelization for HPF compilers tools and libraries loop level optimization automatic data distribution compiler models irregular computation object oriented and functional parallelism

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