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System-level Test and Validation of Hardware/Software Systems



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Victor A. Perevostchikov, Vladimir D. Skoupov

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System-level Test and Validation of Hardware/Software Systems Matteo Sonza Reorda, Zebo Peng, Massimo Violante, 2006-03-30 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities. These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability High Dielectric Constant Materials Howard Huff, David Gilmer, 2005-11-02 Issues relating to the high K gate dielectric are among the greatest challenges for the evolving International Technology Roadmap for Semiconductors ITRS More than just an historical overview this book will assess previous and present approaches related to scaling the gate dielectric and their impact along with the creative directions and forthcoming challenges that will define the future of gate dielectric scaling technology Topics include an extensive review of Moore's Law the classical regime for SiO2 gate dielectrics the transition to silicon oxynitride gate dielectrics the transition to high K gate dielectrics including the drive towards equivalent oxide thickness in the single digit nanometer regime and future directions and issues for ultimate technology generation scaling The vision wisdom and experience of the team of authors will make this book a timely relevant and interesting resource focusing on fundamentals of the 45 nm Technology Generation and beyond Microcontrollers in <u>Practice</u> Ioan Susnea, Marian Mitescu, 2005-07-06 Stressing common characteristics and real applications of the most used microcontrollers this practical guide provides readers with hands on knowledge of how to implement three families of microcontrollers HC11 AVR and 8051 Unlike the rest of the ocean of literature on individual chips Microcontrollers in Practice supplies side by side comparisons and an overview that treats the systems as resources available for implementation Packed with hundreds of practical examples and exercises to foster mastery of concepts and details the guide also includes several extended projects By treating the less expensive 8 bit and RISC microcontrollers this information dense manual equips students and home experimenters with the know how to put these devices into operation *Power Management of* Digital Circuits in Deep Sub-Micron CMOS Technologies Stephan Henzler, 2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and threshold voltages transistor stack forcing and

power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side **Detection and Signal Processing** Wilhelmus Jacobus Witteman, 2007-04-14 This comprehensive monograph deals with detectors signal processors and related noise phenomena Detailed quantitative analyses are developed in a consistent format for thermal detectors vacuum detectors semiconductor detectors and avalanche detectors as well as their accompanying noise currents For signal processing applocations the monograph treats in detail the operational amplifier signal averagers waveform analyzers correlation techniques and heterodyne detection Several original extensions are reported especially for correlation devices and heterodyne detection with noise rejection In addition results of analyses are illustrated with examples of operating systems and of applications in space communication and laser radar Gettering Defects in Semiconductors Victor A. Perevostchikov, Vladimir D. Skoupov, 2005-09-15 Gettering Defects in Semiconductors fulfills three basic purposes to systematize the experience and research in exploiting various gettering techniques in microelectronics and nanoelectronics to identify new directions in research particularly to enhance the perspective of professionals and young researchers and specialists to fill a gap in the contemporary literature on the underlying semiconductor material theory. The authors address not only well established gettering techniques but also describe contemporary trends in gettering technologies from an international perspective The types and properties of structural defects in semiconductors their generating and their transforming mechanisms during fabrication are described The primary emphasis is placed on classifying and describing specific gettering techniques their specificity arising from both their position in a general technological process and the regimes of their application This book addresses both engineers and material scientists interested in semiconducting materials theory and also undergraduate and graduate students in solid state microelectronics and nanoelectronics A comprehensive list of references provides readers with direction for further Continuous-Time Sigma-Delta A/D Conversion Friedel Gerfers, Maurits Ortmanns, 2006-02-27 Sigma delta A reading D converters are a key building block in wireless and multimedia applications This comprehensive book deals with all relevant aspects arising during the analysis design and simulation of the now widespread continuous time implementations of sigma delta modulators The results of several years of research by the authors in the field of CT sigma delta modulators are

covered including the analysis and modeling of different CT modulator architectures CT DT loop filter synthesis a detailed error analysis of all components and possible compensation correction schemes for the non ideal behavior in CT sigma delta modulators Guidance for obtaining low power consumption and several practical implementations are also presented It is shown that all the proposed new theories architectures and possible correction techniques have been confirmed by measurements on discrete or integrated circuits Quantitative results are also provided thus enabling prediction of the resulting accuracy Highly Sensitive Optical Receivers Kerstin Schneider, 2006-11-10 Highly Sensitive Optical Receivers primarily treats the circuit design of optical receivers with external photodiodes Continuous mode and burst mode receivers are compared The monograph first summarizes the basics of III V photodetectors transistor and noise models bit error rate sensitivity and analog circuit design thus enabling readers to understand the circuits described in the main part of the book In order to cover the topic comprehensively detailed descriptions of receivers for optical data communication in general and in particular optical burst mode receivers in deep sub m CMOS are presented Numerous detailed and elaborate illustrations facilitate better understanding High-Dynamic-Range (HDR) Vision Bernd Hoefflinger, 2007-02-16 Creating high fidelity images of our world has been a continuous challenge even as our understanding and skills have evolved The acquisition and mapping of the rich and complex content of visual information rank high among the most demanding technical tasks Now electronic image sensors can record a dynamic range from bright to dark of more than seven orders of magnitude thus exceeding the ability of a human eye by more than a hundred times and displaying five orders of magnitude in brightness resulting in CRT and LCD displays with more than 100 fold improvement This first comprehensive account of high dynamic range HDR vision focusses on HDR real time high speed digital video recording and also systematically presents HDR video transmission and display The power of the eye like logarithmic optoelectronic conversion concept is demonstrated in machine vision medical automotive surveillance and cinematic applications and it is extended to HDR sub retinal implants for the vision impaired While the book conveys the overall picture of HDR vision specific knowledge of microelectronics and image processing is not required It provides a quantitative summary of the major issues to allow the assessment of the state of the art and a glimpse at future developments Selected experts share their know how and expectations in this rapidly evolving art related to the single most powerful of our senses American Book Publishing Record ,2005

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