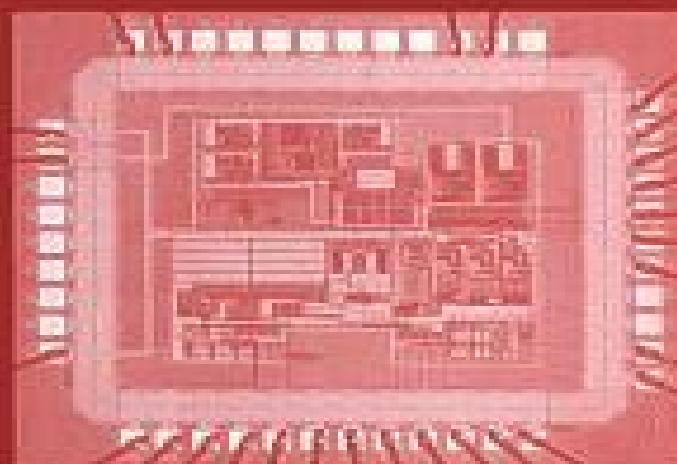


SYSTEMATIC DESIGN OF SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTERS

Ovidiu Bajdechi and Johan H. Huijsing



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Systematic Design Of Sigmadelta Analogtodigital Converters

**Dominique Dallet, José Machado da
Silva**



Systematic Design Of Sigmadelta Analogtodigital Converters:

Systematic Design of Sigma-Delta Analog-to-Digital Converters Ovidiu Bajdechi, Johan Huijsing, 2004-06-01 Systematic Design of Sigma Delta Analog to Digital Converters describes the issues related to the sigma delta analog to digital converters ADCs design in a systematic manner from the top level of abstraction represented by the filters defining signal and noise transfer functions STF NTF passing through the architecture level where topology related performance is calculated and simulated and finally down to parameters of circuit elements like resistors capacitors and amplifier transconductances used in individual integrators The systematic approach allows the evaluation of different loop filters order aggressiveness discrete time or continuous time implementation with quantizers varying in resolution Topologies explored range from simple single loops to multiple cascaded loops with complex structures including more feedbacks and feedforwards For differential circuits with switched capacitor integrators for discrete time DT loop filters and active RC for continuous time CT ones the passive integrator components are calculated and the power consumption is estimated based on top level requirements like harmonic distortion and noise budget This unified systematic approach to choosing the best sigma delta ADC implementation for a given design target yields an interesting solution for a high resolution broadband DSL like ADC operated at low oversampling ratio which is detailed down to transistor level schematics The target audience of Systematic Design of Sigma Delta Analog to Digital Converters are engineers designing sigma delta ADCs and or switched capacitor and continuous time filters both beginners and experienced It is also intended for students academics involved in sigma delta and analog CAD research

Systematic Design of Sigma-delta Analog-to-digital Converters Ovidiu Bajdechi, 2003

Systematic Design of Sigma-Delta Analog-to-Digital Converters Ovidiu Bajdechi, Johan Huijsing, 2004-04-30 Systematic Design of Sigma Delta Analog to Digital Converters describes the issues related to the sigma delta analog to digital converters ADCs design in a systematic manner from the top level of abstraction represented by the filters defining signal and noise transfer functions STF NTF passing through the architecture level where topology related performance is calculated and simulated and finally down to parameters of circuit elements like resistors capacitors and amplifier transconductances used in individual integrators The systematic approach allows the evaluation of different loop filters order aggressiveness discrete time or continuous time implementation with quantizers varying in resolution Topologies explored range from simple single loops to multiple cascaded loops with complex structures including more feedbacks and feedforwards For differential circuits with switched capacitor integrators for discrete time DT loop filters and active RC for continuous time CT ones the passive integrator components are calculated and the power consumption is estimated based on top level requirements like harmonic distortion and noise budget This unified systematic approach to choosing the best sigma delta ADC implementation for a given design target yields an interesting solution for a high resolution broadband DSL like ADC operated at low oversampling ratio which is detailed down to transistor level schematics The target audience of

Systematic Design of Sigma Delta Analog to Digital Converters are engineers designing sigma delta ADCs and or switched capacitor and continuous time filters both beginners and experienced It is also intended for students academics involved in sigma delta and analog CAD research

Systematic Design of CMOS Switched-Current Bandpass Sigma-Delta Modulators for Digital Communication Chips José M. de la Rosa, Belén Pérez-Verdú, Ángel

Rodríguez-Vázquez, 2007-05-08 This very detailed book discusses architectures circuits and procedures for the optimum design of bandpass sigma delta A/D interfaces for mixed signal chips in standard CMOS technologies It provides uniquely in depth coverage of switched current errors which supports the design of high performance SI chips

Sigma Delta A/D Conversion for Signal Conditioning Kathleen Philips, Arthur H.M. van Roermund, 2006-05-05 1 1 Background Moore's Law predicts a decrease by a factor of two in the feature size of CMOS technology every three years and has been valid for years It implies a doubling of the operation speed and a four times higher transistor count per unit of area every three years The combination leads to an eight times higher processing capability per unit of area This ongoing miniaturization allows the integration of complex electronic systems with millions of transistors Very Large Scale Integration and enables the integration of electronic systems An electronic system A generic picture of an integrated electronic system is shown in g 1 1 The heart of the system is the signal processing core This core supports a wide variety of functions such as customization and programmability of multiple applications channel coding the definition of the user interface etc These functions are enabled by DSP a controller CPU and various blocks of memory In advanced ICs these blocks provide almost all signal processing and usually dominate in the overall power and area consumption of integrated systems The huge data rates involved require high speed busses for communication between these blocks A power management unit fuels the system by providing the appropriate supply voltages and currents

Sigma-Delta Converters: Practical Design Guide Jose M. de la Rosa, 2018-08-22

Thoroughly revised and expanded to help readers systematically increase their knowledge and insight about Sigma Delta Modulators Sigma Delta Modulators SDMs have become one of the best choices for the implementation of analog digital interfaces of electronic systems integrated in CMOS technologies Compared to other kinds of Analog to Digital Converters ADCs SDMs cover one of the widest conversion regions of the resolution versus bandwidth plane being the most efficient solution to digitize signals in an increasingly number of applications which span from high resolution low bandwidth digital audio sensor interfaces and instrumentation to ultra low power biomedical systems and medium resolution broadband wireless communications Following the spirit of its first edition Sigma Delta Converters Practical Design Guide 2nd Edition takes a comprehensive look at SDMs their diverse types of architectures circuit techniques analysis synthesis methods and CAD tools as well as their practical design considerations It compiles and updates the current research reported on the topic and explains the multiple trade offs involved in the whole design flow of Sigma Delta Modulators from specifications to chip implementation and characterization The book follows a top down approach in order to provide readers with the necessary

understanding about recent advances trends and challenges in state of the art Ms It makes more emphasis on two key points which were not treated so deeply in the first edition It includes a more detailed explanation of Ms implemented using Continuous Time CT circuits going from system level synthesis to practical circuit limitations It provides more practical case studies and applications as well as a deeper description of the synthesis methodologies and CAD tools employed in the design of converters Sigma Delta Converters Practical Design Guide 2nd Edition serves as an excellent textbook for undergraduate and graduate students in electrical engineering as well as design engineers working on SD data converters who are looking for a uniform and self contained reference in this hot topic With this goal in mind and based on the feedback received from readers the contents have been revised and structured to make this new edition a unique monograph written in a didactical pedagogical and intuitive style

Design of Very High-Frequency Multirate Switched-Capacitor Circuits Ben U Seng Pan,Rui Paulo da Silva Martins,Jose de Albuquerque Epifanio da Franca,2006-07-02 Design of Very High Frequency Multirate Switched Capacitor Circuits presents the theory and the corresponding CMOS implementation of the novel multirate sampled data analog interpolation technique which has its great potential on very high frequency analog frond end filtering due to its inherent dual advantage of reducing the speed of data converters and DSP core together with the specification relaxation of the post continuous time filtering This technique completely eliminates the traditional phenomenon of sampled and hold frequency shaping at the lower input sampling rate Also in order to tackle physical IC imperfections at very high frequency the state of the art circuit design and layout techniques for high speed Switched Capacitor SC circuits are comprehensively discussed Optimum circuit architecture tradeoff analysis Simple speed and power trade off analysis of active elements High order filtering response accuracy with respect to capacitor ratio mismatches Time interleaved effect with respect to gain and offset mismatch Time interleaved effect with respect to timing skew and random jitter with non uniformly holding Stage noise analysis and allocation scheme Substrate and supply noise reduction Gain and offset compensation techniques High bandwidth low power amplifier design and layout Very low timing skew multiphase generation Two tailor made optimum design examples in CMOS are presented The first one achieves a 3 stage 8 fold SC interpolating filter with 5 5MHz bandwidth and 108MHz output sampling rate for a NTSC PAL CCIR 601 digital video at 3 V Another is a 15 tap 57MHz SC FIR bandpass interpolating filter with 4 fold sampling rate increase to 320MHz and the first time embedded frequency band up translation for DDFS system at 2 5V The corresponding chip prototype achieves so far the highest operating frequency highest filter order and highest center frequency with highestdynamic range under the lowest supply voltage when compared to the previously reported high frequency SC filters in CMOS

High-Speed Photodiodes in Standard CMOS

Technology Sasa Radovanovic,Anne-Johan Annema,Bram Nauta,2006-10-11 High speed Photodiodes in Standard CMOS Technology describes high speed photodiodes in standard CMOS technology which allow monolithic integration of optical receivers for short haul communication For short haul communication the cost aspect is important and therefore it is

desirable that the optical receiver can be integrated in the same CMOS technology as the rest of the system. If this is possible then ultimately a single chip system including optical inputs becomes feasible, eliminating EMC and crosstalk problems while data rate can be extremely high. The problem of photodiodes in standard CMOS technology is that they have very limited bandwidth allowing data rates up to only 50 Mbit per second. High speed Photodiodes in Standard CMOS Technology first analyzes the photodiode behaviour and compares existing solutions to enhance the speed. After this the book introduces a new and robust electronic equalizer technique that makes data rates of 3 Gb/s possible without changing the manufacturing technology. The application of this technique can be found in short haul fibre communication optical printed circuit boards but also photodiodes for laser disks.

Matching Properties of Deep Sub-Micron MOS Transistors Jeroen A.

Croon, Willy M Sansen, Herman E. Maes, 2006-06-20 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade off between speed, power, accuracy and yield. Furthermore, due to the down scaling of device dimensions, transistor mismatch has an increasing impact on digital circuits. The matching properties of MOSFETs are studied at several levels of abstraction. A simple and physics based model is presented that accurately describes the mismatch in the drain current. The model is illustrated by dimensioning the unit current cell of a current steering D/A converter. The most commonly used methods to extract the matching properties of a technology are benchmarked with respect to model accuracy, measurement accuracy and speed and physical contents of the extracted parameters. The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied 1 area law. In addition, the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The impact of process parameters on the matching properties is discussed. The impact of gate line edge roughness is investigated, which is considered to be one of the roadblocks to the further down scaling of the MOS transistor. Matching Properties of Deep Sub Micron MOS Transistors is aimed at device physicists, characterization engineers, technology designers, circuit designers or anybody else interested in the stochastic properties of the MOSFET.

Dynamic Characterisation of Analogue-to-Digital Converters Dominique

Dallet, José Machado da Silva, 2006-03-08 The Analogue to digital converter ADC is the most pervasive block in electronic systems. With the advent of powerful digital signal processing and digital communication techniques, ADCs are fast becoming critical components for system's performance and flexibility. Knowing accurately all the parameters that characterise their dynamic behaviour is crucial, on one hand, to select the most adequate ADC architecture and characteristics for each end application and on the other hand, to understand how they affect performance bottlenecks in the signal processing chain. Dynamic Characterisation of Analogue to Digital Converters presents a state of the art overview of the methods and procedures employed for characterising ADCs dynamic performance behaviour using sinusoidal stimuli. The three classical

methods histogram sine wave fitting and spectral analysis are thoroughly described and new approaches are proposed to circumvent some of their limitations This is a must have compendium which can be used by both academics and test professionals to understand the fundamental mathematics underlining the algorithms of ADC testing and as an handbook to help the engineer in the most important and critical details for their implementation

Reviewing **Systematic Design Of Sigmadelta Analogtodigital Converters**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is truly astonishing. Within the pages of "**Systematic Design Of Sigmadelta Analogtodigital Converters**," an enthralling opus penned by a very acclaimed wordsmith, readers attempt an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve into the book's central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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