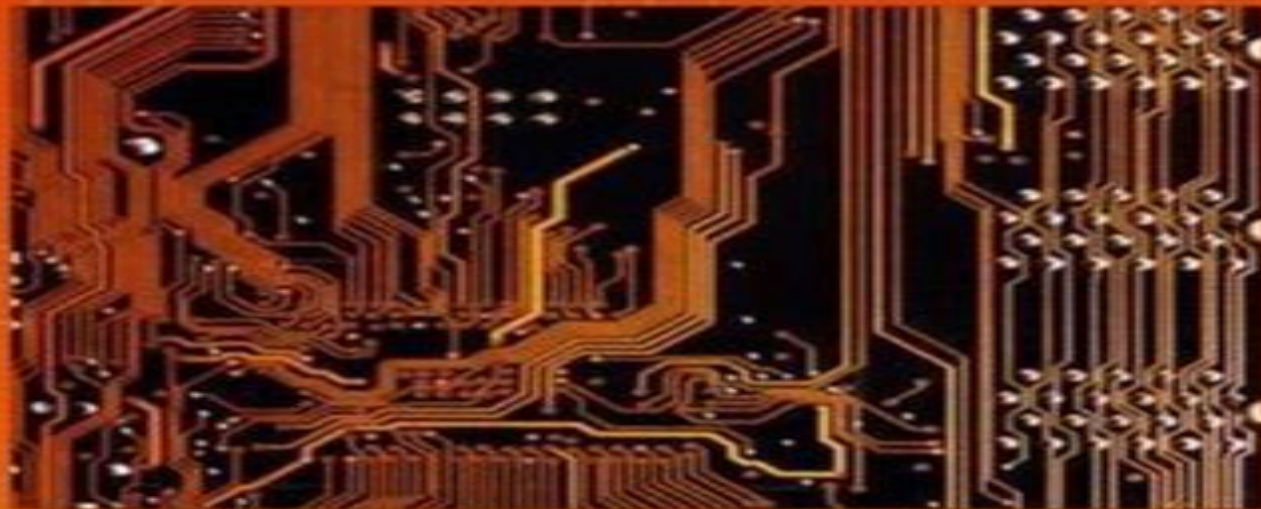# Symbolic Analysis and Reduction of VLSI Circuits

Chung-Kuan Cheng, Zhanhai Qin and Sheldon Tan

Symbolic Analysis And Reduction Of Vlsi Circuits

Angsuman Sarkar,Swapnadip De,Manash Chanda,Chandan Kumar Sarkar

Symbolic Analysis And Reduction Of Vlsi Circuits:

  Symbolic Analysis and Reduction of VLSI Circuits Zhanhai Qin,Chung-Kuan Cheng,2009-03-13 Symbolic analysis is an intriguing topic in VLSI designs The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation However analyzing circuits symbolically remains a challenging research issue Therefore in this book we survey the recent results as the progress of on going works rather than as the solution of the field For parasitic reduction we approximate a huge amount of electrical parameters into a simplified RLC network This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time A symbolic analysis approach reduces the circuit according to the network topology Thus the designer can maintain the meaning of the original network and perform the analysis hierarchically For analog circuit designs symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit The analysis allows us to optimize the circuit behavior The book is divided into three parts Part I touches on the basics of circuit analysis in time domain and in s domain For an s domain expression the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform On the other hand the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain Part II focuses on the techniques for parasitic reduction In Chapter 2 we present the approximation methods to match the first few moments with reduced circuit orders In Chapter 3 we apply the Y Delta transformation to reduce the dynamic linear network The method finds the exact values of the low order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments In Chapter 4 we handle two major issues of the Y Delta transformation common factors in fractional expressions and round off errors Chapter 5 explains the stability of the reduced expression in particular the Ruth Hurwitz Criterion We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks In Chapter 6 we present techniques to synthesize circuits to approximate the reduced expressions after the transformation In Part III we discuss symbolic generation of the determinants and cofactors for the application to analog designs In Chapter 7 we depict the classical topological analysis approach In Chapter 8 we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation In Chapter 9 we take only significant terms when we search through determinant decision diagram to approximate the solution In Chapter 10 we extend the determinant decision diagram to a hierarchical model The construction of the modules through the hierarchy is similar to the Y Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator Therefore we describe the method to prune the common factors   **Symbolic Analysis and Reduction of VLSI Circuits** Qin Zhanhai,Chung-Kuan Cheng,2008-11-01 Symbolic analysis is an intriguing topic in VLSI designs The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation However analyzing circuits symbolically remains a challenging research issue Therefore in this book we survey the recent results as the progress

of on going works rather than as the solution of the field For parasitic reduction we approximate a huge amount of electrical parameters into a simplified RLC network This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time A symbolic analysis approach reduces the circuit according to the network topology Thus the designer can maintain the meaning of the original network and perform the analysis hierarchically For analog circuit designs symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit The analysis allows us to optimize the circuit behavior The book is divided into three parts Part I touches on the basics of circuit analysis in time domain and in s domain For an s domain expression the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform On the other hand the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain Part II focuses on the techniques for parasitic reduction In Chapter 2 we present the approximation methods to match the first few moments with reduced circuit orders In Chapter 3 we apply the Y Delta transformation to reduce the dynamic linear network The method finds the exact values of the low order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments In Chapter 4 we handle two major issues of the Y Delta transformation common factors in fractional expressions and round off errors Chapter 5 explains the stability of the reduced expression in particular the Ruth Hurwitz Criterion We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks In Chapter 6 we present techniques to synthesize circuits to approximate the reduced expressions after the transformation In Part III we discuss symbolic generation of the determinants and cofactors for the application to analog designs In Chapter 7 we depict the classical topological analysis approach In Chapter 8 we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation In Chapter 9 we take only significant terms when we search through determinant decision diagram to approximate the solution In Chapter 10 we extend the determinant decision diagram to a hierarchical model The construction of the modules through the hierarchy is similar to the Y Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator Therefore we describe the method to prune the common factors *Advanced Symbolic Analysis for VLSI Systems* Guoyong Shi,Sheldon X.-D. Tan,Esteban Tlelo Cuautle,2014-06-19 This book provides comprehensive coverage of the recent advances in symbolic analysis techniques for design automation of nanometer VLSI systems The presentation is organized in parts of fundamentals basic implementation methods and applications for VLSI design Topics emphasized include statistical timing and crosstalk analysis statistical and parallel analysis performance bound analysis and behavioral modeling for analog integrated circuits Among the recent advances the Binary Decision Diagram BDD based approaches are studied in depth The BDD based hierarchical symbolic analysis approaches have essentially broken the analog circuit size barrier *Advanced Model Order Reduction Techniques in VLSI Design* Sheldon Tan,Lei He,2007-05-31 Model order reduction MOR techniques reduce the complexity of VLSI

designs paving the way to higher operating speeds and smaller feature sizes This book presents a systematic introduction to and treatment of the key MOR methods employed in general linear circuits using real world examples to illustrate the advantages and disadvantages of each algorithm Following a review of traditional projection based techniques coverage progresses to more advanced MOR methods for VLSI design including HMOR passive truncated balanced realization TBR methods efficient inductance modeling via the VPEC model and structure preserving MOR techniques Where possible numerical methods are approached from the CAD engineer s perspective avoiding complex mathematics and allowing the reader to take on real design problems and develop more effective tools With practical examples and over 100 illustrations this book is suitable for researchers and graduate students of electrical and computer engineering as well as practitioners working in the VLSI design industry **Advances in Analog Circuits** Esteban Tlelo-Cuautle,2011-02-02 This book highlights key design issues and challenges to guarantee the development of successful applications of analog circuits Researchers around the world share acquired experience and insights to develop advances in analog circuit design modeling and simulation The key contributions of the sixteen chapters focus on recent advances in analog circuits to accomplish academic or industrial target specifications <u>Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs</u> Ruijing Shen,Sheldon X.-D. Tan,Hao Yu,2014-07-08 Since process variation and chip performance uncertainties have become more pronounced as technologies scale down into the nanometer regime accurate and efficient modeling or characterization of variations from the device to the architecture level have become imperative for the successful design of VLSI chips This book provides readers with tools for variation aware design methodologies and computer aided design CAD of VLSI systems in the presence of process variations at the nanometer scale It presents the latest developments for modeling and analysis with a focus on statistical interconnect modeling statistical parasitic extractions statistical full chip leakage and dynamic power analysis considering spatial correlations statistical analysis and modeling for large global interconnects and analog mixed signal circuits Provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of VLSI systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits Helps chip designers understand the potential and limitations of their design tools improving their design productivity Presents analysis of each algorithm with practical applications in the context of real circuit design Includes numerical examples for the quantitative analysis and evaluation of algorithms presented Provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of VLSI systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits Helps chip designers understand the potential and limitations of their design tools improving their design productivity Presents analysis of each algorithm with practical applications in thecontext of real circuit design Includes numerical examples for the quantitative analysis and evaluation of algorithms presented *Computer-Aided Design of Analog Integrated Circuits and Systems* Rob A.

Rutenbar,Georges G. E. Gielen,2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck *VLSI: Systems on a Chip* Luis Miguel Silveira,Srinivas Devadas,Ricardo A. Reis,2013-11-11 For over three decades now silicon capacity has steadily been doubling every year and a half with equally staggering improvements continuously being observed in operating speeds This increase in capacity has allowed for more complex systems to be built on a single silicon chip Coupled with this functionality increase speed improvements have fueled tremendous advancements in computing and have enabled new multi media applications Such trends aimed at integrating higher levels of circuit functionality are tightly related to an emphasis on compactness in consumer electronic products and a widespread growth and interest in wireless communications and products These trends are expected to persist for some time as technology and design methodologies continue to evolve and the era of Systems on a Chip has definitely come of age While technology improvements and spiraling silicon capacity allow designers to pack more functions onto a single piece of silicon they also highlight a pressing challenge for system designers to keep up with such amazing complexity To handle higher operating speeds and the constraints of portability and connectivity new circuit techniques have appeared Intensive research and progress in EDA tools design methodologies and techniques is required to empower designers with the ability to make efficient use of the potential offered by this increasing silicon capacity and complexity and to enable them to design test verify and build such systems **Computational Intelligence in Analog and Mixed-Signal (AMS) and Radio-Frequency (RF) Circuit Design** Mourad Fakhfakh,Esteban Tlelo-Cuautle,Patrick Siarry,2015-07-14 This book explains the application of recent advances in computational intelligence algorithms design methodologies and synthesis techniques to the design of integrated circuits and systems It highlights new biasing and sizing approaches and optimization

techniques and their application to the design of high performance digital VLSI radio frequency and mixed signal circuits and systems This first of two related volumes addresses the design of analog and mixed signal AMS and radio frequency RF circuits with 17 chapters grouped into parts on analog and mixed signal applications and radio frequency design It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits **Advanced VLSI Design and Testability Issues** Suman Lata Tripathi,Sobhit Saxena,Sushanta Kumar Mohapatra,2020-08-19 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC s structure and function which makes it much more difficult to reverse engineer 1992 IEEE International Symposium on Circuits and Systems Stanley A. White,Institute of Electrical and Electronics Engineers,1992 ISCAS 98 provides the latest results on many important subjects in computer aided design modeling and simulation testing signal processing neural and fuzzy systems multimedia image and video processing linear and nonlinear circuits and systems and many more exciting fields **Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology** Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit

Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **Pathological Elements in Analog Circuit Design** Mourad Fakhfakh,Marian Pierzchala,2018-03-23 This book is a compilation and a collection of tutorials and recent advances in the use of nullors combinations of nullators and norators and pathological mirrors in analog circuit and system design It highlights the basic theory trends and challenges in the field making it an excellent reference resource for researchers and designers working in the synthesis analysis and design of analog integrated circuits With its tutorial character it can also be used for teaching Singular elements such as nullors and pathological mirrors can arguably be considered as universal blocks since they can represent all existing analog building blocks and they allow complex integrated circuits to be designed simply and effectively These pathological elements are now used in a wide range of applications in modern circuit system theory and also in design practice **Advanced Model Reduction and Simulation Techniques for Integrated Electronic and Thermal Circuits** Pu Liu,2008 **Algorithms and Data Structures in VLSI Design** Christoph Meinel,Thorsten Theobald,2012-12-06 One of the main problems in chip design is the huge number of possible combinations of individual chip elements leading to a combinatorial explosion as chips become more complex New key results in theoretical computer science and in the design of data structures and efficient algorithms can be applied fruitfully here The application of ordered binary decision diagrams OBDDs has led to dramatic performance improvements in many computer aided design projects This textbook provides an introduction to the foundations of this interdisciplinary research area with an emphasis on applications in computer aided circuit design and formal verification Low Power VLSI Design Angsuman Sarkar,Swapnadip De,Manash Chanda,Chandan Kumar Sarkar,2016-08-08 This book teaches basic and advanced concepts new methodologies and recent developments in VLSI technology with a focus on low power design It provides insight on how to use Tanner Spice Cadence tools Xilinx tools VHDL programming and Synopsis to design simple and complex circuits using latest state of the art technologies Emphasis is placed on fundamental transistor circuit level design

concepts   The Summary of Engineering Research University of Illinois at Urbana-Champaign. Office of Engineering Publications,1984   **Digest of Technical Papers** ,1987   1989 IEEE International Symposium on Circuits and Systems ,1989   **Trade-Offs in Analog Circuit Design** Chris Toumazou,George S. Moschytz,Barrie Gilbert,2007-05-08 As the frequency of communication systems increases and the dimensions of transistors are reduced more and more stringent performance requirements are placed on analog circuits This is a trend that is bound to continue for the foreseeable future and while it does understanding performance trade offs will constitute a vital part of the analog design process It is the insight and intuition obtained from a fundamental understanding of performance conflicts and trade offs that ultimately provides the designer with the basic tools necessary for effective and creative analog design Trade offs in Analog Circuit Design which is devoted to the understanding of trade offs in analog design is quite unique in that it draws together fundamental material from and identifies interrelationships within a number of key analog circuits The book covers ten subject areas Design methodology Technology General Performance Filters Switched Circuits Oscillators Data Converters Transceivers Neural Processing and Analog CAD Within these subject areas it deals with a wide diversity of trade offs ranging from frequency dynamic range and power gain bandwidth speed dynamic range and phase noise to tradeoffs in design for manufacture and IC layout The book has by far transcended its original scope and has become both a designer s companion as well as a graduate textbook An important feature of this book is that it promotes an intuitive approach to understanding analog circuits by explaining fundamental relationships and in many cases providing practical illustrative examples to demonstrate the inherent basic interrelationships and trade offs Trade offs in Analog Circuit Design draws together 34 contributions from some of the world s most eminent analog circuits and systems designers to provide for the first time a comprehensive text devoted to a very important and timely approach to analog circuit design

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