

Optimizing Parallel Programs with Explicit Synchronization

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Abstract: We present compiler analyses and optimizations for explicitly parallel programs that communicate through a shared address space. Any type of code motion on explicitly parallel programs requires a new kind of analysis to ensure that operations reordered on one processor cannot be observed by another. The analysis, based on work by Shasha and Snir, checks for cycles among interfering accesses. We improve the accuracy of their analysis by using additional information from post-wait synchronization, barriers, and locks.

We demonstrate the use of this analysis by optimizing remote access on distributed memory machines. The optimizations include message pipelining, to allow multiple outstanding remote memory operations, conversion of two-way to one-way communication, and elimination of communication through data re-use. The performance improvements are as high as 20-35% for programs running on a CM-5 multiprocessor using the Split-C language as a global address layer.

1 Introduction

Optimizing explicitly parallel shared memory programs requires new types of static analysis to ensure that accesses reordered on one processor cannot be observed by another. Intuitively, the parallel programmer relies on the notion of *sequential consistency*: the parallel execution must behave as if it were an interleaving of the sequences of memory operations from each of the processors [12]. If only the local dependencies within a processor are observed, the program execution might not be sequentially consistent [13]. To guarantee sequential consistency under reordering transformations, a new type of analysis called *cycle detection* is required [18].

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Figure 1: If the read of *Flag* returns 1, the read of *Data* should see the new value.

An example to illustrate sequential consistency is shown in Figure 1. The program is indeterminate in that the read of *Flag* may return either 0 or 1, and if it is 0, then the read of *Data* may return either 0 or 1. However, if 1 has been read from *Flag*, then 1 must be the result of the read from *Data*. If the two program fragments were analyzed by a sequential compiler, it might determine that the reads or writes could be reordered, since there are no local dependencies. If either pair of the accesses is reordered, the execution in which *Flag* is 1 and *Data* is 0, might result.

Even if the compiler does not reorder the shared memory accesses, reordering may take place at many levels in a multiprocessor system. At the processor level, a superscalar may issue an instruction as soon as all its operands are available, so writes to different locations might be issued in the order the values become available. Most processors have write buffers, which allow read operations to overtake write operations that have been issued earlier. In fact, on the SuperSparcs [20] the write-buffer itself is not guaranteed to be FIFO. Reordering may also take place at the network level in distributed memory multiprocessors, because some networks adaptively route packets to avoid congestion. Even if packets do not get reordered, two access sent to two different processors may be handled out of order, since latencies may vary. Also, on a machine like DASH [13], with hardware caching, writes do not wait for all invalidations to complete, so remote accesses might appear to execute in reverse-order. These architectural features usually come with support to ensure sequential consistency, such as a memory barrier or a write-buffer flush to enforce ordering between memory operations, or a test for completion of a remote operation. However, these new instructions must be inserted by the compiler. If a standard uniprocessor compiler is used for generating code, these special instructions would not be automatically inserted.

The cycle detection problem is to detect access cycles, such as the one designated by the figure-right in Figure 1. In

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web iv year 12 and 13 examinations the two examinations are high stake summative assessments to gauge the students achievement after 12 and 13 years of schooling assess the level of competency at that level for selection of students to higher and tertiary institutions and prospective employment e examinations

year 13 national examination provisional results - Feb 09 2023

web jan 28 2021 media centre news year 13 national examination provisional results year 13 national examination provisional results 28 01 2021 the ministry education heritage and arts will release the year 13 national examination provisional results on friday 29 january 2021

college of engineering science technology - Dec 07 2022

web jun 9 2023 notice quarter 3 2023 examination cest quarter 3 2023 final exam timetable updated on 06 09 2023