
Switch-Level Timing Simulation of MOS VLSI Circuits

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Kluwer Academic Publishers

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Switchlevel Timing Simulation Of Mos Vlsi Circuits:

Switch-Level Timing Simulation of MOS VLSI Circuits Vasant B. Rao, David V. Overhauser, Timothy N. Trick, Ibrahim N. Hajj, 2012-12-06 Only two decades ago most electronic circuits were designed with a slide rule and the designs were verified using breadboard techniques. Simulation tools were a research curiosity and in general were mistrusted by most designers and test engineers. In those days the programs were not user friendly, models were inadequate and the algorithms were not very robust. The demand for simulation tools has been driven by the increasing complexity of integrated circuits and systems and it has been aided by the rapid decrease in the cost of computing that has occurred over the past several decades. Today a wide range of tools exist for analysis, design and verification and expert systems and synthesis tools are rapidly emerging. In this book only one aspect of the analysis and design process is examined but it is a very important aspect that has received much attention over the years. It is the problem of accurate circuit and timing simulation. **Switch-level Timing**

Simulation of MOS VLSI Circuits Vasant Bangalore Rao, 1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors. Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits. The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well. The algorithms presented in this report have been implemented in a computer program called MOSTIM. In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed. Author **Digital Timing Macromodeling for VLSI**

Design Verification Jeong-Taek Kong, David V. Overhauser, 2012-12-06 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques. It presents detailed discussion of the various techniques implemented in circuit timing: fast timing, switch level timing, switch level and gate level simulation. It also discusses mixed mode simulation and interconnection analysis methods. The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels. The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels. Specifically the techniques address the device model detail: transistor coupling capacitance, effective channel length modulation, series transistor reduction, effective transconductance, input terminal dependence, gate parasitic capacitance, the body effect, the impact of parasitic RC interconnects and the effect of transmission gates. The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers. The techniques presented in Chapters 4-6 can be implemented in other macromodels and are demonstrated using the

macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques *Electrothermal Analysis of VLSI Systems* Yi-Kan Cheng, Ching-Han Tsai, Chin-Chi Teng, Sung-Mo (Steve) Kang, 2005-12-01 This useful book addresses electrothermal problems in modern VLSI systems It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires The authors present three important applications of VLSI electrothermal analysis temperature dependent electromigration diagnosis cell level thermal placement and temperature driven power and timing analysis **Switch-Level Timing Simulation of MOS VLSI**

(Metal-Oxide-Semiconductor Very Large-Scale Integrated) Circuits Vasant B. Rao, ILLINOIS UNIV AT URBANA COORDINATED SCIENCE LAB., 1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well The algorithms presented in this report have been implemented in a computer program called MOSTIM In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed Author *Mixed-Mode Simulation and Analog Multilevel Simulation* Resve A. Saleh, Shyh-Jye Jou, A. Richard Newton, 2013-03-09 Mixed Mode Simulation and Analog Multilevel Simulation addresses the problems of simulating entire mixed analog digital systems in the time domain A complete hierarchy of modeling and simulation methods for analog and digital circuits is described Mixed Mode Simulation and Analog Multilevel Simulation also provides a chronology of the research in the field of mixed mode simulation and analog multilevel simulation over the last ten to fifteen years In addition it provides enough information to the reader so that a prototype mixed mode simulator could be developed using the algorithms in this book Mixed Mode Simulation and Analog Multilevel Simulation can also be used as documentation for the SPLICE family of mixed mode programs as they are based on the algorithms and techniques described in this book *Mixed-Mode Simulation* Resve A. Saleh, A. Richard Newton, 2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques

described in this book and so it can also serve as documentation for these programs

ACKNOWLEDGEMENTS The authors would like to dedicate this book to Prof D O Pederson for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discussions and collaborations with Jim Kleckner Young Kim Alberto Sangiovanni Vincentelli and Jacob White and we thank them for their contributions We also thank the countless others who participated in the research work and read early versions of this book Lillian Beck provided many useful suggestions to improve the manuscript Yun cheng Ju did the artwork for the illustrations

Analog Design Issues in Digital VLSI Circuits and Systems Juan J. Becerra, Eby G. Friedman, 2012-12-06 Analog Design Issues in Digital VLSI Circuits and Systems brings together in one place important contributions and up to date research results in this fast moving area Analog Design Issues in Digital VLSI Circuits and Systems serves as an excellent reference providing insight into some of the most challenging research issues in the field

Hierarchical Modeling for VLSI Circuit Testing Debashis Bhattacharya, John P. Hayes, 2012-12-06 Test generation is one of the most difficult tasks facing the designer of complex VLSI based digital systems Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology It has long been recognized that the testing problem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation however the development of such methods has proceeded very slowly To be acceptable high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line SSL fault model which is tightly bound to the gate level of abstraction This monograph presents a novel approach to solving the foregoing problem It is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals A circuit is viewed as a collection of high level components such as adders multiplexers and registers interconnected by n bit buses To match this high level circuit model we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel However by reducing the bus size from n to one we can obtain the traditional gate level circuit and models

Models for Large Integrated Circuits Patrick DeWilde, Zhen-Qiu Ning, 2012-12-06 A modern microelectronic circuit can be compared to a large construction a large city on a very small area A memory chip a DRAM may have up to 64 million bit locations on a surface of a few square centimeters Each new generation of integrated circuit generations are measured by factors of four in overall complexity requires a substantial increase in density from the current technology added precision a decrease of the size of geometric features and an increase in the total usable surface The microelectronic industry has set the trend Ultra large funds have been invested in the construction of new plants to produce the ultra large scale circuits with utmost precision under the most severe conditions The decrease in feature size to submicrons 0.7 micron is quickly becoming available does not only bring

technological problems New design problems arise as well The elements from which microelectronic circuits are build transistors and interconnects have different shape and behave differently than before Phenomena that could be neglected in a four micron technology such as the non uniformity of the doping profile in a transistor or the mutual capacitance between two wires now play an important role in circuit design This situation does not make the life of the electronic designer easier he has to take many more parasitic effects into account up to the point that his ideal design will not function as originally planned

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