SO/ CIRCUIT DESIGN CONCEPTS

Kerry Bernstein Norman J. Rohrer

IBM Microelectronics



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primarily concerned with circuit related issues It considers SOI material in terms of implementation that is promising or has been used elsewhere in circuit development with historical perspective where appropriate An International Standard Dynamic RAM Muzaffer A. Siddigi, 2017-12-19 Because of their widespread use Model for SOI Circuit Design Pin Su,2002 in mainframes PCs and mobile audio and video devices DRAMs are being manufactured in ever increasing volume both in stand alone and in embedded form as part of a system on chip Due to the optimum design of their components access transistor storage capacitor and peripherals DRAMs are the cheapest and densest semiconductor memory currently available As a result most of DRAM structure research and development focuses on the technology used for its constituent components and their interconnections However only a few books are available on semiconductor memories in general and fewer on DRAMs Dynamic RAM Technology Advancements provides a holistic view of the DRAM technology with a systematic description of the advancements in the field since the 1970s and an analysis of future challenges Topics Include DRAM cells of all types including planar three dimensional 3 D trench or stacked COB or CUB vertical and mechanically robust cells using advanced transistors and storage capacitors Advancements in transistor technology for the RCAT SCAT FinFET BT FinFET Saddle and advanced recess type and storage capacitor realizations How sub 100 nm trench DRAM technologies and sub 50 nm stacked DRAM technologies and related topics may lead to new research Various types of leakages and power consumption reduction methods in active and sleep mode Various types of SAs and yield enhancement techniques employing ECC and redundancy A worthwhile addition to semiconductor memory research academicians and researchers interested in the design and optimization of high density and cost efficient DRAMs may also find it useful as part of a graduate level course

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Nanoelectronics Balwinder Raj, Suman Lata Tripathi, Tarun Chaudhary, Mandeep Singh, 2025-05-15 This book exhibits a unique way of explaining nanomaterials and devices and analyzing their design parameters to meet the sub nanoregime challenges for low power chip design Since process variability device sizing and power supply scaling are

ongoing challenges in very large scale integration VLSI circuit designs this book highlights the conventional and novel nanomaterials devices and circuits leakage current mitigation techniques and other important trade offs along with exhaustive analysis More focus has been placed throughout the book on various trade offs for high speed and low power VLSI devices and circuits co design This book Discusses advanced nano semiconductor devices such as FinFET nanowires tunnel field effect transistors carbon nanotube field effect transistors and high electron mobility transistors Presents high performance semiconductor devices at nanoscale technology nodes for the analysis of quantum effects and their impact on circuits and systems Covers power dissipation and reduction techniques for high performance devices Explains both silicon and non silicon devices for various applications like digital logic and analog radio frequency applications Examines the difficulties and practical design approaches for extremely low power analog integrated circuits It is primarily written for senior undergraduates graduate students and academic researchers in the fields of electrical engineering electronics and communications engineering materials science nanoscience and nanotechnology Nanoscale CMOS VLSI Circuits: **Design for Manufacturability** Sandip Kundu, Aswin Sreedhar, 2010-06-22 Cutting Edge CMOS VLSI Design for Manufacturability Techniques This detailed guide offers proven methods for optimizing circuit designs to increase the yield reliability and manufacturability of products and mitigate defects and failure Covering the latest devices technologies and processes Nanoscale CMOS VLSI Circuits Design for Manufacturability focuses on delivering higher performance and lower power consumption Costs constraints and computational efficiencies are also discussed in the practical resource Nanoscale CMOS VLSI Circuits covers Current trends in CMOS VLSI design Semiconductor manufacturing technologies Photolithography Process and device variability analyses and modeling Manufacturing Aware Physical Design Closure Metrology manufacturing defects and defect extraction Defect impact modeling and yield improvement techniques Physical design and reliability DFM tools and methodologies

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