Overall framework of SRAM-based CIM

Circuit level:
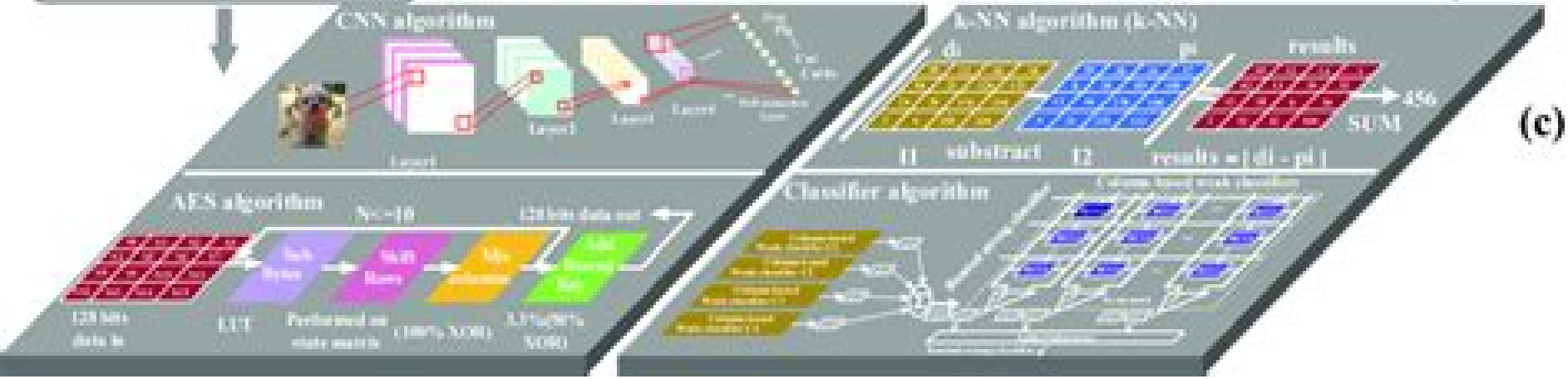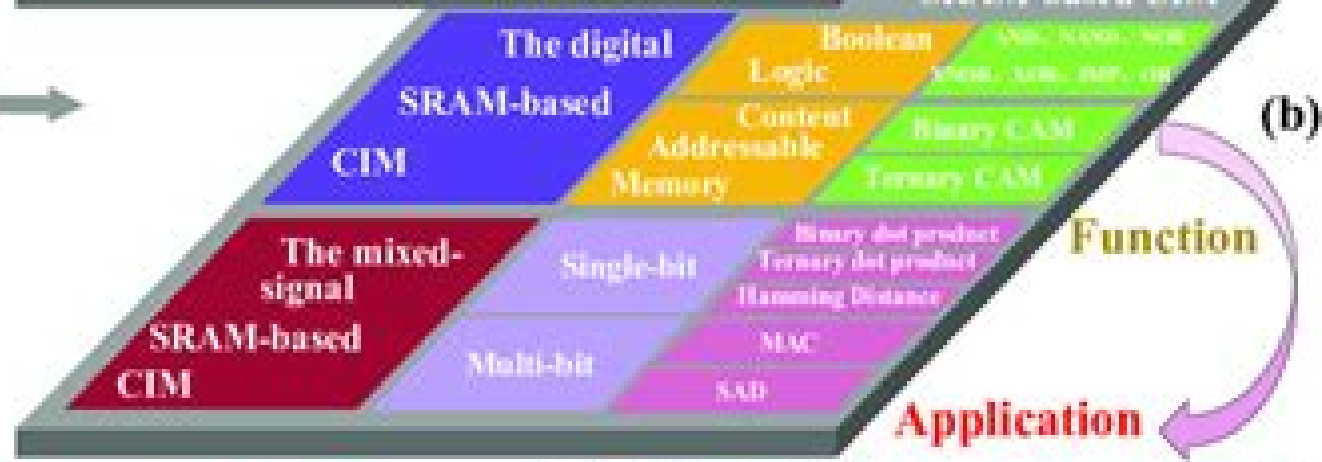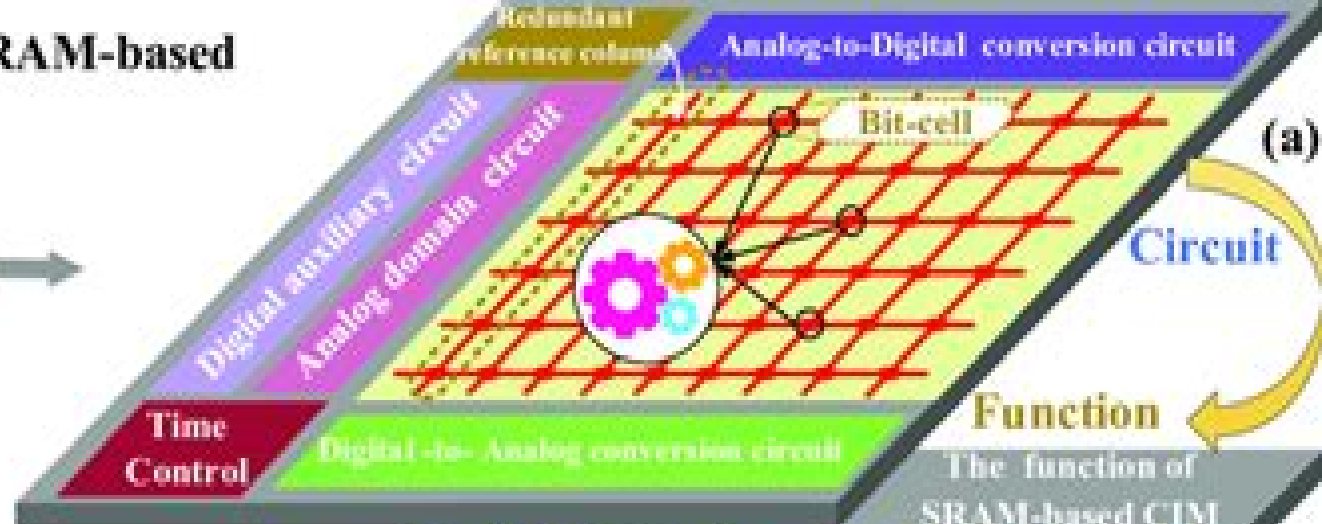① Bitcell structures
② Peripheral circuits

Function level:
① Digital CIM
② Mixed-signal CIM

Application level:
① CNN ③ k-NN
② AES ④ Classifier

(a)

Redundant reference column

Analog-to-Digital conversion circuit

Bit-cell

Digital auxiliary circuit

Analog domain circuit

Time Control

Digital -to- Analog conversion circuit

Circuit

Function

The function of SRAM-based CIM

(b)

The digital SRAM-based CIM

Boolean Logic

Content Addressable Memory

XNR, NAND, NOR, XNOR, XOR, IMP, OR

Binary CAM

Ternary CAM

The mixed-signal SRAM-based CIM

Single-bit

Binary dot product
Ternary dot product
Hamming Distance

Multi-bit

MAC

SAD

Function

Application

(c)

CNN algorithm

Layer

k-NN algorithm (k-NN)

di

pi

results

456

SUM

t1 substract t2

results = | di - pi |

AES algorithm

Nr=10

128 bits data out

128 bits data in

LUT

Perhormed on state matrix

(100% XOR)

3.3%@90% XOR)

Classifier algorithm

Testing Static Random Access Memories

Alberto Bosio,Luigi Dilillo,Patrick Girard,Serge Pravossoudovitch,Arnaud Virazel

Testing Static Random Access Memories:

  Testing Static Random Access Memories Said Hamdioui,2004-03-31 Embedded memories are one of the fastest growing segments oftoday s new technology market According to the 2001 InternationalTechnology Roadmap for Semiconductors embedded memories will continueto dominate the increasing system on chip SoC content in the nextseveral years approaching 94% of the SoC area in about 10 years Furthermore the shrinking size of manufacturing structures makesmemories more sensitive to defects Consequently the memory yieldwill have a dramatic impact on the overall Defect per million level hence on the overall SoC yield Meeting a high memory yield requiresunderstanding memory designs modeling their faulty behaviors designing adequate tests and diagnosis algorithms as well as efficientself test and repair schemes Testing Static Random Access Memories covers testing of one ofthe important semiconductor memories types it address testing ofstatic random access memories SRAMs both single port andmulti port It contributes to the technical acknowledge needed bythose involved in memory testing engineers and researchers The bookbegins with outlining the most popular SRAMs architectures Then thedescription of realistic fault models based on defect injection andSPICE simulation are introduced Thereafter high quality and lowcost test patterns as well as test strategies for single port two port and any p port SRAMs are presented together with somepreliminary test results showing the importance of the new tests inreducing DPM level The impact of the port restrictions e g read only ports on the fault models tests and test strategies isalso discussed Features   *High Performance Memory Testing* R. Dean Adams,2005-12-29 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author s 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested   *Advanced Test Methods for SRAMs* Alberto Bosio,Luigi Dilillo,Patrick Girard,Serge Pravossoudovitch,Arnaud Virazel,2009-10-08 Modern electronics depend on nanoscaled technologies that present new challenges in terms of testing and diagnostics Memories are particularly prone to defects since they exploit the technology limits to get the highest density This book is an invaluable guide to the testing and diagnostics of the latest generation of SRAM one of the most widely applied types of memory Classical methods for testing memory are designed to handle the so called static faults but these test solutions are not sufficient for faults that are emerging in the latest Very Deep Sub Micron VDSM technologies These new fault models referred to as dynamic faults are not covered by classical test solutions and require the dedicated test sequences presented in this book   Digital Logic Testing and Simulation Alexander Miczo,2003-10-10 Your road map for meeting today s digital testing challenges Today

digital logic devices are common in products that impact public safety including applications in transportation and human implants Accurate testing has become more critical to reliability safety and the bottom line Yet as digital systems become more ubiquitous and complex the challenge of testing them has become more difficult As one development group designing a RISC stated the work required to test a chip of this size approached the amount of effort required to design it A valued reference for nearly two decades Digital Logic Testing and Simulation has been significantly revised and updated for designers and test engineers who must meet this challenge There is no single solution to the testing problem Organized in an easy to follow sequential format this Second Edition familiarizes the reader with the many different strategies for testing and their applications and assesses the strengths and weaknesses of the various approaches The book reviews the building blocks of a successful testing strategy and guides the reader on choosing the best solution for a particular application Digital Logic Testing and Simulation Second Edition covers such key topics as Binary Decision Diagrams BDDs and cycle based simulation Tester architectures Standard Test Interface Language STIL Practical algorithms written in a Hardware Design Language HDL Fault tolerance Behavioral Automatic Test Pattern Generation ATPG The development of the Test Design Expert TDX the many obstacles encountered and lessons learned in creating this novel testing approach Up to date and comprehensive Digital Logic Testing and Simulation is an important resource for anyone charged with pinpointing faulty products and assuring quality safety and profitability **Digital Timing Measurements** Wolfgang Maichen,2006-10-03 As many circuits and applications now enter the Gigahertz frequency range accurate digital timing measurements have become crucial in the design verification characterization and application of electronic circuits To be successful in this endeavour an engineer needs a knowledge base covering instrumentation measurement techniques signal integrity jitter and timing concepts and statistics Very often even the most experienced digital test engineers while mastering some of those subjects lack systematic knowledge or experience in the high speed signal area Digital Timing Measurements gives a compact practice oriented overview on all those subjects The emphasis is on useable concepts and real life guidelines that can be readily put into practice with references to the underlying mathematical theory It unites in one place a variety of information relevant to high speed testing measurement signal fidelity and instrumentation **Emerging Nanotechnologies** Mohammad Tehranipoor,2007-12-08 Emerging Nanotechnologies Test Defect Tolerance and Reliability covers various technologies that have been developing over the last decades such as chemically assembled electronic nanotechnology Quantum dot Cellular Automata QCA and nanowires and carbon nanotubes Each of these technologies offers various advantages and disadvantages Some suffer from high power some work in very low temperatures and some others need indeterministic bottom up assembly These emerging technologies are not considered as a direct replacement for CMOS technology and may require a completely new architecture to achieve their functionality Emerging Nanotechnologies Test Defect Tolerance and Reliability brings all of these issues together in one place for readers and researchers who are interested in this rapidly changing field **VLSI**

Test Principles and Architectures Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures **New Methods of Concurrent Checking** Michael Gössel,Vitaly Ocheretny,Egor Sogomonyan,Daniel Marienfeld,2008-04-26 Computers are everywhere around us We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation Computers are incredibly fast inexpensive and equipped with almost unimag able large storage capacity Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the world can be 2 easily accommodated on an ordinary chip The size of such a chip is less than 1 cm This is a fantastic achievement for an unbelievably low price However the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future Can we always trust computers Are computers always reliable Are chips suf ciently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by c current checking Besides permanent faults many temporary or transient faults are also to be expected **Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits** Manoj Sachdev,José Pineda de Gyvez,2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent **Defect Oriented Testing for CMOS Analog and Digital Circuits** Manoj Sachdev,2013-06-29 Defect oriented testing is expected to play a

significant role in coming generations of technology Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches Furthermore with increased level of integration an IC may contain diverse building blocks Such blocks include digital logic PLAs volatile and non volatile memories and analog interfaces For such diverse building blocks traditional fault modeling and test approaches will become increasingly inadequate Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits ICs have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject It is essential reading for all design and test professionals as well as researchers and students working in the field A strength of this book is its breadth Types of designs considered include analog and digital circuits programmable logic arrays and memories Having a fault model does not automatically provide a test Sometimes design for testability hardware is necessary Many design for testability ideas supported by experimental evidence are included from the Foreword by Vishwani D Agrawal **Introduction to VLSI Systems** Ming-Bo Lin,2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding of circuit and layout design issues Furthermore engineers can often develop their physical intuition to estimate the behavior of circuits rapidly without relying predominantly on computer aided design CAD tools Introduction to VLSI Systems A Logic Circuit and System Perspective addresses the need for teaching such a topic in terms of a logic circuit and system design perspective To achieve the above mentioned goals this classroom tested book focuses on Implementing a digital system as a full custom integrated circuit Switch logic design and useful paradigms that may apply to various static and dynamic logic families The fabrication and layout designs of complementary metal oxide semiconductor CMOS VLSI Important issues of modern CMOS processes including deep submicron devices circuit optimization interconnect modeling and optimization signal integrity power integrity clocking and timing power dissipation and electrostatic discharge ESD Introduction to VLSI Systems builds an understanding of integrated circuits from the bottom up paying much attention to logic circuit layout and system designs Armed with these tools readers can not only comprehensively understand the features and limitations of modern VLSI technologies but also have enough background to adapt to this ever changing field *System-on-Chip Test Architectures* Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics

testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students   9th International Conference on Robotic, Vision, Signal Processing and Power Applications Haidi Ibrahim,Shahid Iqbal,Soo Siang Teoh,Mohd Tafir Mustaffa,2016-09-29 The proceeding is a collection of research papers presented at the 9th International Conference on Robotics Vision Signal Processing Power Applications ROVISP 2016 by researchers scientists engineers academicians as well as industrial professionals from all around the globe to present their research results and development activities for oral or poster presentations The topics of interest are as follows but are not limited to Robotics Control Mechatronics and Automation Vision Image and Signal Processing Artificial Intelligence and Computer Applications Electronic Design and Applications Telecommunication Systems and Applications Power System and Industrial Applications Engineering Education   **VLSI Design and Test** S. Rajaram,N.B. Balamurugan,D. Gracia Nirmala Rani,Virendra Singh,2019-01-24 This book constitutes the refereed proceedings of the 22st International Symposium on VLSI Design and Test VDAT 2018 held in Madurai India in June 2018 The 39 full papers and 11 short papers presented together with 8 poster papers were carefully reviewed and selected from 231 submissions The papers are organized in topical sections named digital design analog and mixed signal design hardware security micro bio fluidics VLSI testing analog circuits and devices network on chip memory quantum computing and NoC sensors and interfaces   **Industrial Engineering and Applications** L.-C. Tang,2023-08-09 The field of industrial engineering IE has a very wide scope from production processes and automation to supply chain management but the scope of IE techniques has expanded beyond the traditional domains of application and is now relevant to areas that matter most to society at large This book presents the proceedings of ICIEA 2023 the 10th International Conference on Industrial Engineering and Applications held in Phuket Thailand from 4 to 6 April

2023 The conference was conducted in hybrid mode with close to 100 delegates attending in person and about 50 participants attending online A total of 272 submissions were received for the conference of which 120 were accepted for presentation with 83 of those published here as full papers These papers cover a wide range of topics within the scope of industrial and systems engineering including but not limited to supply chain and logistics quality and reliability advanced manufacturing and production scheduling to ergonomics and man machine systems interfaces In particular a significant number of papers are devoted to machine learning techniques and applications beyond the traditional manufacturing sector to include healthcare sustainability assessment and other social issues Offering an overview of recent research and novel applications the book will be of interest to all those whose work involves the application of industrial engineering techniques

VLSI-SoC: Opportunities and Challenges Beyond the Internet of Things Michail Maniatakos,Ibrahim (Abe) M. Elfadel,Matteo Sonza Reorda,H. Fatih Ugurdag,José Monteiro,Ricardo Reis,2019-05-16 This book contains extended and revised versions of the best papers presented at the 25th IFIP WG 10 5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2017 held in Abu Dhabi United Arab Emirates in August 2017 The 11 papers included in this book were carefully reviewed and selected from the 33 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the latest scientific and industrial results and developments as well as future trends in the field of System on Chip SoC Design On the occasion of the silver jubilee of the VLSI SoC conference series the book also includes a special chapter that presents the history of the VLSI SoC series of conferences and its relation with VLSI SoC evolution since the early 80s up to the present *Mathematical and Engineering Methods in Computer Science* Antonin Kucera,Thomas A. Henzinger,Jaroslav Nešetřil,Tomas Vojnar,David Antos,2013-01-17 This volume contains the post proceedings of the 8th Doctoral Workshop on Mathematical and Engineering Methods in Computer Science MEMICS 2012 held in Znojmo Czech Republic in October 2012 The 13 thoroughly revised papers were carefully selected out of 31 submissions and are presented together with 6 invited papers The topics covered by the papers include computer aided analysis and verification applications of game theory in computer science networks and security modern trends of graph theory in computer science electronic systems design and testing and quantum information processing **Quality and Reliability of Technical Systems** Alessandro Birolini,2013-03-14 High reliability maintainability and safety are expected from complex equipment and systems To build these characteristics into an item failure rate and failure mode analyses have to be performed early in the design phase starting at the com ponent level and have to be supported by a set of design guidelines for reliability and maintainability as well as by extensive design reviews Before production qualification tests of prototypes must ensure that quality and reliability targets have been reached In the production phase processes and procedures have to be selec ted and monitored to assure the required quality level For many systems availabi lity requirements must also be satisfied In these cases stochastic processes can be used to investigate and optimize availability

including logistical support This book presents the state of the art of the methods and procedures necessary for a cost and time effective quality and reliability assurance during the design and production of equipment and systems It takes into consideration that 1 Quality and reliability assurance of complex equipment and systems requires that all engineers involved in a project undertake a set of specific activities from the definition to the operating phase which are performed concurrently to achieve the best performance quality and reliability for given cost and time schedule targets **Testing Semiconductor Memories** A. J. van de Goor,1991 Comprehensive coverage of memory test problems at chip array and board level is provided in this book For each of these test levels a class of fault models is introduced along with tests for these models The author also presents algorithms of relevant fault models together with proofs of their correctness Special attention is given to why a fault model belongs to a particular class and why it is of interest A software package suitable for use on IBM PCs and compatibles is also available which consists of a set of memory test programs and a simulation package demonstrating how the algorithms are executed and the relationship of the algorithm with the memory Analog Circuit Design Johan Huijsing,Rudy J. van de Plassche,Willy M.C. Sansen,2013-03-14 Johan H Huijsing This book contains 18 tutorial papers concentrated on 3 topics each topic being covered by 6 papers The topics are Low Noise Low Power Low Voltage Mixed Mode Design with CAD Tools Voltage Current and Time References The papers of this book were written by top experts in the field currently working at leading European and American universities and companies These papers are the reviewed versions of the papers presented at the Workshop on Advances in Analog Circuit Design which was held in Villach Austria 26 28 April 1995 The chairman of the Workshop was Dr Franz Dielacher from Siemens Austria The program committee existed of Johan H Huijsing from the Delft University of Technology Prof Willy Sansen from the Catholic University of Leuven and Dr Rudy 1 van der Plassche from Philips Eindhoven This book is the fourth of aseries dedicated to the design of analog circuits The topics which were covered earlier were Operational Amplifiers Analog to Digital Converters Analog Computer Aided Design Mixed AlD Circuit Design Sensor Interface Circuits Communication Circuits Low Power Low Voltage Integrated Filters Smart Power As the Workshop will be continued year by year a valuable series of topics will be built up from all the important areas of analog circuit design I hope that this book will help designers of analog circuits to improve their work and to speed it up

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