SOC DESIGN METHODOLOGIES

Edited by
Michel Robert
Bruno Rouzeyre
Christian Piguet
Marie-Lise Flottes

Soc Design Methodologies

Christian Piguet,Ricardo Reis,Dimitrios Soudris

Soc Design Methodologies:

SOC Design Methodologies Michel Robert,Bruno Rouzeyre,Christian Piguet,Marie-Lise Flottes,2013-03-15 The 11 th IFIP International Conference on Very Large Scale Integration in Montpellier France December 3 5 2001 was a great success The main focus was about IP Cores Circuits and System Designs 55 years ago in late 1947 the transistor was invented and everybody knows that it was by William Shockley John Bardeen and Walter H Brattein Bell Telephone Laboratories which received the Nobel Prize in Physics in 1956 Probably everybody thinks that it was recognized immediately as a major invention **VLSI-SoC: Design Methodologies for SoC and SiP** Christian Piguet,Ricardo Reis,Dimitrios Soudris,2010-04-08 This book contains extended and revised versions of the best papers that were p sented during the 16th edition of the IFIP IEEE WG10 5 International Conference on Very Large Scale Integration a global System on a Chip Design CAD conference The 16th conference was held at the Grand Hotel of Rhodes Island Greece October 13 15 2008 Previous conferences have taken place in Edinburgh Trondheim V couver Munich Grenoble Tokyo Gramado Lisbon Montpellier Darmstadt Perth Nice and Atlanta VLSI SoC 2008 was the 16th in a series of international conferences sponsored by IFIP TC 10 Working Group 10 5 and IEEE CEDA that explores the state of the art and the new developments in the field of VLSI systems and their designs The purpose of the conference was to provide a forum to exchange ideas and to present industrial and research results in the fields of VLSI ULSI systems embedded systems and croelectronic design and test **A Platform-Centric Approach to System-on-Chip (SOC) Design** Vijay Madisetti,Chonlameth Arpnikanondt,2006-06-28 Increasing system complexity has created a pressing need for better design tools and associated methodologies and languages for meeting the stringent time to market and cost constraints Platform centric and platfo based system on chip SoC design methodologies based on reuse of software and hardware functionality has also gained increasing exposure and usage within the Electronic System Level ESL design communities The book proposes a new methodology for realizing platform centric design of complex systems and presents a detailed plan for its implementation The proposed plan allows component vendors system integrators and product developers to collaborate effectively and efficiently to create complex products within budget and schedule constraints This book focuses more on the use of platforms in the design of products and not on the design of platforms themselves Platform centric design is not for everyone as some may feel that it does not allow them to differentiate their offering from competitors to a significant degree However its proponents may claim that the time market and cost advantages of platform centric design more than compensate for any drawbacks *A Practical Approach to VLSI System on Chip (SoC) Design* Veena S. Chakravarthi,2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure

requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs **From ASICs to SOCs** Farzad Nekoogar,Faranak Nekoogar,2003 From ASICs to SOCs A Practical Approach by Farzad Nekoogar and Faranak Nekoogar covers the techniques principles and everyday realities of designing ASICs and SOCs Material includes current issues in the field front end and back end designs integration of IPs on SOC designs and low power design techniques and methodologies Appropriate for practicing chip designers as well as graduate students in electrical engineering

Correct-by-Construction Approaches for SoC Design Roopak Sinha,Parthasarathi Roop,Samik Basu,2013-08-23 This book describes an approach for designing Systems on Chip such that the system meets precise mathematical requirements The methodologies presented enable embedded systems designers to reuse intellectual property IP blocks from existing designs in an efficient reliable manner automatically generating correct SoCs from multiple possibly mismatching components

System-on-Chip Methodologies & Design Languages Peter J. Ashenden,Jean Mermet,Ralf Seepold,2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field Advances in Design Methods from Modeling Languages for Embedded Systems and SoC's Dominique Borrione,2010-08-24 More than ever FDL is the place for researchers developers industry designers academia and EDA tool companies to present and to learn about the latest scientific achievements practical applications and users experiences in the domain of specification and design languages FDL covers the modeling and design methods and their latest supporting tools for complex embedded systems systems on chip and heterogeneous systems FDL 2009 is the twelfth in a series of events that were held all over Europe in selected locations renowned for their Universities and Reseach Institutions as well as the importance of their industrial environment in Computer Science and Micro electronics In 2009 FDL was organized in the attractive south of France area of Sophia Antipolis together with the DASIP Design and Architectures for Signal and Image Processing Conference and the SAME Sophia Antipolis MicroElectronics Forum All submitted papers were carefully reviewed to build a program with 27 full and 10 short contributions From these the Program Committee selected a shorter list based on the evaluations of the reviewers and the originality and relevance of the work that was presented at the Forum The revised and sometimes extended versions of

these contributions constitute the chapters of this volume Advances in Design Methods from Modeling Languages for Embedded Systems and SoC s presents extensions to standard specification and description languages as well as new language based design techniques and methodologies to solve the challenges raised by mixed signal and multi processor systems on a chip It is intended as a reference for researchers and lecturers as well as a state of the art milestone for designers and CAD developers **VLSI Circuit Design Methodology Demystified** Liming Xiu,2007-10-23 This book was written to arm engineers qualified and knowledgeable in the area of VLSI circuits with the essential knowledge they need to get into this exciting field and to help those already in it achieve a higher level of proficiency Few people truly understand how a large chip is developed but an understanding of the whole process is necessary to appreciate the importance of each part of it and to understand the process from concept to silicon It will teach readers how to become better engineers through a practical approach of diagnosing and attacking real world problems **VLSI-SOC: From Systems to Chips** Manfred Glesner,Ricardo Reis,Leandro Indrusiak,Vincent Mooney,Hans Eveking,2006-08-16 This book contains extended and revised versions of the best papers that have been presented during the twelfth edition of the IFIP TC10 WG10 5 International Conference on Very Large Scale Integration a Global System on a Chip Design CAD Conference The 12 edition was held at the Lufthansa Training Center in Seeheim Jugenheim south of Darmstadt Germany December 1 3 2003 Previous conferences have taken place in Edinburgh 81 Trondheim 83 Tokyo 85 Vancouver 87 Munich 89 Edinburgh 91 Grenoble 93 Tokyo 95 Gramado 97 Lisbon 99 andMontpellier 01 The purpose of this conference sponsored by IFIP TC 10 Working Group 10 5 is to provide a forum to exchange ideas and show research results in the field of microelectronics design The current trend toward increasing chip integration brings about exhilarating new challenges both at the physical and system design levels this conference aims to address these exciting new issues The 2003 edition of VLSI SoC conserved the traditional structure which has been successful in previous editions The quality of submissions 142 papers made the selection process difficult but finally 57 papers and 14 posters were accepted for presentation in VLSI SoC 2003 Submissions came from Austria Bulgaria Brazil Canada Egypt England Estonia Finland France Germany Greece Hungary India Iran Israel Italy Japan Korea Malaysia Mexico Netherlands Poland Portugal Romania Spain Sweden Taiwan and the United States of America From 57 papers presented at the conference 18 were selected to have an extended and revised version included in this book **The Simple Art of SoC Design** Michael Keating, Synopsys Fellow,2011-05-17 This book tackles head on the challenges of digital design in the era of billion transistor SoCs It discusses fundamental design concepts in design and coding required to produce robust functionally correct designs It also provides specific techniques for measuring and minimizing complexity in RTL code Finally it discusses the tradeoff between RTL and high level C based design and how tools and languages must progress to address the needs of tomorrow s SoC designs **Component Design by Example** Ben Cohen,2001 **Reuse Methodology Manual for System-On-A-Chip Designs** Pierre Bricaud,2013-03-09 Silicon technology now allows us to build chips consisting of tens of

millions of transistors This technology promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant while design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process From the Foreword Synopsys and Mentor Graphics have joined forces to help make IP reuse a reality One of the goals of our Design Reuse Partnership is to develop demonstrate and document a reuse based design methodology that works The Reuse Manual RMM is the result of this effort Aart J de Geus Synopsys Inc Walden C Rhines Mentor Graphics Corporation   <u>Mixed-Signal Methodology Guide</u> Jess Chen,Michael Henrie,Monte F. Mar, Ph.D.,Mladen Nizic,2012 This book the Mixed signal Methodology Guide Advanced Methodology for AMS IP and SoC Design Verification and Implementation provides a broad overview of the design verification and implementation methodologies required for today s mixed signal designs The book covers mixed signal design trends and challenges abstraction of analog using behavioral models assertion based metric driven verification methodology applied on analog and mixed signal and verification of low power intent in mixed signal design It also describes methodology for physical implementation in context of concurrent mixed signal design and for handling advanced node physical effects The book contains many practical examples of models and techniques The authors believe it should serve as a reference to many analog digital and mixed signal designers verification physical implementation engineers and managers in their pursuit of information for a better methodology required to address the challenges of modern mixed signal design   **Reuse Methodology Manual** Pierre Bricaud,2012-12-06 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant even as design complexities grow Tools are

not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process Reuse Methodology Manual for System On A Chip Designs Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high quality SoC designs **Retargetable Processor System Integration into Multi-Processor System-on-Chip Platforms** Andreas Wieferink,Heinrich Meyr,Rainer Leupers,2008-07-08 This book presents a methodology and the associated tooling for enabling design space exploration as well as a successive refinement flow for the design of optimized MP SoCs with a high degree of automation **Reuse Methodology Manual for System-on-a-Chip Designs** Michael Keating,Pierre Bricaud,2002 Reuse Methodology Manual for System on a Chip Designs Third Edition outlines a set of best practices for creating reusable designs for use in an SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world Silicon and tool technologies move so quickly that many of the details of design for reuse will undoubtedly continue to evolve over time But the fundamental aspects of the methodology described in this book have become widely adopted and are likely to form the foundation of chip design for some time to come Development methodology necessarily differs between system designers and processor designers as well as between DSP developers and chipset developers However there is a common set of problems facing everyone who is designing complex chips In response to these problems design teams have adopted a block based design approach that emphasizes design reuse Reusing macros sometimes called cores that have already been designed and verified helps to address all of the problems above However in adopting reuse based design design teams have run into a significant problem Reusing blocks that have not been explicitly designed for reuse has often provided little or no benefit to the team The effort to integrate a pre existing block into new designs can become prohibitively high if the block does not provide the right views the right documentation and the right functionality From this experience design teams have realized that reuse based design requires an explicit methodology for developing reusable macros that are easy to integrate into SoC designs This manual focuses on describing these techniques Features of the Third Edition Up to date State of the art Reuse as a solution for circuit designers A chronicle of best practices All chapters updated and revised Generic guidelines non tool specific Emphasis on hard IP and physical design **Signal Integrity Effects in Custom IC and ASIC Designs** Raminderpal Singh,2001-12-12 offers a

tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity Jake Buurma Senior Vice President Worldwide Research Development Cadence Design Systems Inc Covers signal integrity effects in high performance Radio Frequency RF IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future A Wiley IEEE Press publication

Designing SOCs with Configured Cores Steve Leibson,2006-08-15 Microprocessor cores used for SOC design are the direct descendents of Intel s original 4004 microprocessor Just as packaged microprocessor ICs vary widely in their attributes so do microprocessors packaged as IP cores However SOC designers still compare and select processor cores the way they previously compared and selected packaged microprocessor ICs The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades This assumption is no longer valid Processor cores for SOC designs can be far more plastic than microprocessor ICs for board level system designs Shaping these cores for specific applications produces much better processor efficiency and much lower system clock rates Together Tensilica s Xtensa and Diamond processor cores constitute a family of software compatible microprocessors covering an extremely wide performance range from simple control processors to DSPs to 3 way superscalar processors Yet all of these processors use the same software development tools so that programmers familiar with one processor in the family can easily switch to another This book emphasizes a processor centric MPSOC multiple processor SOC design style shaped by the realities of the 21st century and nanometer silicon It advocates the assignment of tasks to firmware controlled processors whenever possible to maximize SOC flexibility cut power dissipation reduce the size and number of hand built logic blocks shrink the associated verification effort and minimize the overall design risk An essential no nonsense guide to the design of 21st century mega gate SOCs using nanometer silicon Discusses today s key issues affecting SOC design based on author s decades of personal experience in developing large digital systems as a design engineer while working at Hewlett Packard s Desktop Computer Division and at EDA workstation pioneer Cadnetix and covering such topics as an award winning technology journalist and editor in chief for EDN magazine and the Microprocessor Report Explores conventionally accepted boundaries and perceived limits of processor based system design and then explodes these artificial constraints through a fresh outlook on and discussion of the special abilities of processor cores designed specifically for SOC design Thorough exploration of the evolution of processors and processor cores used for ASIC and SOC design with a look at where the industry has come from and where it s going Easy to understand explanations of the capabilities of configurable and extensible processor cores through a detailed examination of Tensilica s configurable extensible Xtensa processor core and six pre configured Diamond cores The most comprehensive assessment available of the practical aspects of configuring and using multiple processor cores to achieve very difficult and ambitious SOC price performance and power design goals

Formal Methods for Industrial Critical Systems Gwen Salaün,Bernhard Schätz,2011-09-19 This book constitutes the

proceedings of the 16th International Workshop on Formal Methods for Industrial Critical Systems FMICS 2011 held in Trento Italy in August 2011 The 16 papers presented together with 2 invited talks were carefully reviewed and selected from 39 submissions The aim of the FMICS workshop series is to provide a forum for researchers who are interested in the development and application of formal methods in industry It also strives to promote research and development for the improvement of formal methods and tools for industrial applications

Soc Design Methodologies Book Review: Unveiling the Power of Words

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