Switch-Level Timing Simulation of MOS VLSI Circuits

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Switch-Level Timing Simulation of MOS VLSI Circuits Vasant B. Rao,David V. Overhauser,Timothy N. Trick,Ibrahim N. Hajj,2012-12-06 Only two decades ago most electronic circuits were designed with a slide rule and the designs were verified using breadboard techniques Simulation tools were a research curiosity and in general were mistrusted by most designers and test engineers In those days the programs were not user friendly models were inadequate and the algorithms were not very robust The demand for simulation tools has been driven by the increasing complexity of integrated circuits and systems and it has been aided by the rapid decrease in the cost of com puting that has occurred over the past several decades Today a wide range of tools exist for analYSiS deSign and verification and expert systems and synthesis tools are rapidly emerging In this book only one aspect of the analysis and design process is examined but it is a very important aspect that has received much attention over the years It is the problem of accurate circuit and timing simulation **Switch-level Timing Simulation of MOS VLSI Circuits** Vasant Bangalore Rao,1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well The algorithms presented in this report have been implemented in a computer program called MOSTIM In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed Author *Digital Timing Macromodeling for VLSI Design Verification* Jeong-Taek Kong,David V. Overhauser,2012-12-06 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the

macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques   Electrothermal Analysis of VLSI Systems Yi-Kan Cheng,Ching-Han Tsai,Chin-Chi Teng,Sung-Mo (Steve) Kang,2005-12-01 This useful book addresses electrothermal problems in modern VLSI systems It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires The authors present three important applications of VLSI electrothermal analysis temperature dependent electromigration diagnosis cell level thermal placement and temperature driven power and timing analysis   Switch-Level Timing Simulation of MOS VLSI (Metal-Oxide-Semiconductor Very Large-Scale Integrated) Circuits Vasant B. Rao,ILLINOIS UNIV AT URBANA COORDINATED SCIENCE LAB.,1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well The algorithms presented in this report have been implemented in a computer program called MOSTIM In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed Author   Mixed-Mode Simulation and Analog Multilevel Simulation Resve A. Saleh,Shyh-Jye Jou,A. Richard Newton,2013-03-09 Mixed Mode Simulation and Analog Multilevel Simulation addresses the problems of simulating entire mixed analog digital systems in the time domain A complete hierarchy of modeling and simulation methods for analog and digital circuits is described Mixed Mode Simulation and Analog Multilevel Simulation also provides a chronology of the research in the field of mixed mode simulation and analog multilevel simulation over the last ten to fifteen years In addition it provides enough information to the reader so that a prototype mixed mode simulator could be developed using the algorithms in this book Mixed Mode Simulation and Analog Multilevel Simulation can also be used as documentation for the SPLICE family of mixed mode programs as they are based on the algorithms and techniques described in this book   Mixed-Mode Simulation Resve A. Saleh,A. Richard Newton,2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques

described in this book and so it can also serve as docu mentation for these programs ACKNOWLEDGEMENTS The authors would like to dedicate this book to Prof D O Peder son for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discus sions and collaborations with Jim Kleckner Young Kim Alberto Sangiovanni Vincentelli and Jacob White and we thank them for their contributions We also thank the countless others who participated in the research work and read early versions of this book Lillian Beck provided many useful suggestions to improve the manuscript Yun cheng Ju did the artwork for the illustrations **Analog Design Issues in Digital VLSI Circuits and Systems** Juan J. Becerra,Eby G. Friedman,2012-12-06 Analog Design Issues in Digital VLSI Circuits and Systems brings together in one place important contributions and up to date research results in this fast moving area Analog Design Issues in Digital VLSI Circuits and Systems serves as an excellent reference providing insight into some of the most challenging research issues in the field **Hierarchical Modeling for VLSI Circuit Testing** Debashis Bhattacharya,John P. Hayes,2012-12-06 Test generation is one of the most difficult tasks facing the designer of complex VLSI based digital systems Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology It is long been recognized that the testing prob lem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation however the development of such methods has proceeded very slowly To be acceptable high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line SSL fault model which is tightly bound to the gate level of abstraction This monograph presents a novel approach to solving the foregoing problem It is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals A circuit is viewed as a collection of high level components such as adders multiplexers and registers interconnected by n bit buses To match this high level circuit model we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel However by reducing the bus size from n to one we can obtain the traditional gate level circuit and models **Models for Large Integrated Circuits** Patrick DeWilde,Zhen-Qiu Ning,2012-12-06 A modern microelectronic circuit can be compared to a large construction a large city on a very small area A memory chip a DRAM may have up to 64 million bit locations on a surface of a few square centimeters Each new generation of integrated circuit generations are measured by factors of four in overall complexity requires a substantial increase in density from the current technology added precision a decrease of the size of geometric features and an increase in the total usable surface The microelectronic industry has set the trend Ultra large funds have been invested in the construction of new plants to produce the ultra large scale circuits with utmost precision under the most severe conditions The decrease in feature size to submicrons 0 7 micron is quickly becoming availabl does

not only bring technological problems New design problems arise as well The elements from which microelectronic circuits are build transistors and interconnects have different shape and behave differently than before Phenomena that could be neglected in a four micron technology such as the non uniformity of the doping profile in a transistor or the mutual capacitance between two wires now play an important role in circuit design This situation does not make the life of the electronic designer easier he has to take many more parasitic effects into account up to the point that his ideal design will not function as originally planned   Gallium Arsenide Digital Circuits Omar Wing,2012-12-06 Gallium Arsenide technology has come of age GaAs integrated circuits are available today as gate arrays with an operating speed in excess of one Gigabits per second Special purpose GaAs circuits are used in optical fiber digital communications systems for the purpose of regeneration multiplexing and switching of the optical signals As advances in fabrication and packaging techniques are made the operat ing speed will further increase and the cost of production will reach a point where large scale application of GaAs circuits will be economical in these and other systems where speed is paramount This book is written for students and engineers who wish to enter into this new field of electronics for the first time and who wish to embark on a serious study of the subject of GaAs circuit design No prior knowledge of GaAs technology is assumed though some previous experience with MOS circuit design will be helpful A good part of the book is devoted to circuit analysis to the extent that is possible for non linear circuits The circuit model of the GaAs transistor is derived from first principles and analytic formulas useful in predicting the approxi mate circuit performance are also derived Computer simulation is used throughout the book to show the expected performance and to study the effects of parameter variations   **Steady-State Methods for Simulating Analog and Microwave Circuits** Kenneth S. Kundert,Jacob K. White,Alberto L. Sangiovanni-Vincentelli,2013-03-09 The motivation for starting the work described in this book was the interest that Hewlett Packard s microwave circuit designers had in simulation techniques that could tackle the problem of finding steady state solutions for nonlinear circuits particularly circuits containing distributed elements such as transmission lines Examining the problem of computing steady state solutions in this context has led to a collection of novel numerical algorithms which we have gathered along with some background material into this book Although we wished to appeal to as broad an audience as possible to treat the subject in depth required maintaining a narrow focus Our compromise was to assume that the reader is familiar with basic numerical methods such as might be found in dahlquist74 or vlach83 but not assume any specialized knowledge of methods for steady state problems Although we focus on algorithms for computing steady state solutions of analog and microwave circuits the methods herein are general in nature and may find use in other disciplines A number of new algorithms are presented the contributions primarily centering around new approaches to harmonic balance and mixed frequency time methods These methods are described along with appropriate background material in what we hope is a reasonably satisfying blend of theory practice and results The theory is given so that the algorithms can be fully understood and their correctness

established   **Testing and Reliable Design of CMOS Circuits** Niraj K. Jha,Sandip Kundu,2012-12-06 In the last few years CMOS technology has become increas ingly dominant for realizing Very Large Scale Integrated VLSI circuits The popularity of this technology is due to its high den sity and low power requirement The ability to realize very com plex circuits on a single chip has brought about a revolution in the world of electronics and computers However the rapid advance ments in this area pose many new problems in the area of testing Testing has become a very time consuming process In order to ease the burden of testing many schemes for designing the circuit for improved testability have been presented These design for testability techniques have begun to catch the attention of chip manufacturers The trend is towards placing increased emphasis on these techniques Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults In order to take care of this problem we need to build fault tolerant systems The area of fault tolerant computing has steadily gained in importance Today many universities offer courses in the areas of digital system testing and fault tolerant computing Due to the impor tance of CMOS technology a significant portion of these courses may be devoted to CMOS testing This book has been written as a reference text for such courses offered at the senior or graduate level Familiarity with logic design and switching theory is assumed The book should also prove to be useful to professionals working in the semiconductor industry   **Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies** Zhong Yuan Chong,Willy M.C. Sansen,2013-03-09 Analog circuit design has grown in importance because so many circuits cannot be realized with digital techniques Examples are receiver front ends particle detector circuits etc Actually all circuits which require high precision high speed and low power consumption need analog solutions High precision also needs low noise Much has been written already on low noise design and optimization for low noise Very little is available however if the source is not resistive but capacitive or inductive as is the case with antennas or semiconductor detectors This book provides design techniques for these types of optimization This book is thus intended firstly for engineers on senior or graduate level who have already designed their first operational amplifiers and want to go further It is especially for engineers who do not want just a circuit but the best circuit Design techniques are given that lead to the best performance within a certain technology Moreover this is done for all important technologies such as bipolar CMOS and BiCMOS Secondly this book is intended for engineers who want to understand what they are doing The design techniques are intended to provide insight In this way the design techniques can easily be extended to other circuits as well Also the design techniques form a first step towards design automation Thirdly this book is intended for analog design engineers who want to become familiar with both bipolar and CMOS technologies and who want to learn more about which transistor to choose in BiCMOS   *Iterative Identification and Restoration of Images* Reginald L. Lagendijk,Jan Biemond,2012-12-06 One of the most intriguing questions in image processing is the problem of recovering the desired or perfect image from a degraded version In many instances one has the feeling that the degradations in the image are such that relevant information is close to being recognizable if

only the image could be sharpened just a little This monograph discusses the two essential steps by which this can be achieved namely the topics of image identification and restoration More specifically the goal of image identifi cation is to estimate the properties of the imperfect imaging system blur from the observed degraded image together with some statistical char acteristics of the noise and the original uncorrupted image On the basis of these properties the image restoration process computes an estimate of the original image Although there are many textbooks addressing the image identification and restoration problem in a general image processing setting there are hardly any texts which give an indepth treatment of the state of the art in this field This monograph discusses iterative procedures for identifying and restoring images which have been degraded by a linear spatially invari ant blur and additive white observation noise As opposed to non iterative methods iterative schemes are able to solve the image restoration problem when formulated as a constrained and spatially variant optimization prob In this way restoration results can be obtained which outperform the lem results of conventional restoration filters   *Subband Image Coding* John W. Woods,2013-06-29 This book concerns a new method of image data compression which weil may supplant the well established block transfonn methods that have been state of the art for the last 15 years Subband image coding or SBC was first perfonned as such in 1985 and as the results became known at first through conference proceedings and later through journal papers the research community became excited about both the theoretical and practical aspects of this new approach This excitement is continuing today with many major research laboratories and research universities around the world investigating the subband approach to coding of color images high resolution images video including video conferencing and advanced tele vision and the medical application of picture archiving systems Much of the fruits of this work is summarized in the eight chapters of this book which were written by leading practitioners in this field The subband approach to image coding starts by passing the image through a two or three dimensional filter bank The two dimensional 2 D case usually is hierarchical consisting of two stages of four filters each Thus the original image is split into 16 subband images with each one decimated or subsampled by 4x4 resulting in a data conservation The individual channel data is then quantized for digital transmission In an attractive variation an octave like approach herein tenned subband pyramid is taken for the decomposition resulting in a total of just eleven subbands

   Nonlinear Digital Filters Ioannis Pitas,Anastasios N. Venetsanopoulos,2013-03-14 The function of a filter is to transform a signal into another one more suit able for a given purpose As such filters find applications in telecommunica tions radar sonar remote sensing geophysical signal processing image pro cessing and computer vision Numerous authors have considered deterministic and statistical approaches for the study of passive active digital multidimen sional and adaptive filters Most of the filters considered were linear although the theory of nonlinear filters is developing rapidly as it is evident by the numerous research papers and a few specialized monographs now available Our research interests in this area created opportunity for cooperation and co authored publications during the past few years in many nonlinear filter families

described in this book As a result of this cooperation and a visit from John Pitas on a research leave at the University of Toronto in September 1988 the idea for this book was first conceived The difficulty in writing such a mono graph was that the area seemed fragmented and no general theory was available to encompass the many different kinds of filters presented in the literature However the similarities of some families of nonlinear filters and the need for such a monograph providing a broad overview of the whole area made the pro ject worthwhile The result is the book now in your hands typeset at the Department of Electrical Engineering of the University of Toronto during the summer of 1989 **Algorithmic and Register-Transfer Level Synthesis: The System Architect's Workbench** Donald E. Thomas,Elizabeth D. Lagnese,Robert A. Walker,Jayanth V. Rajan,Robert L. Blackburn,John A. Nestor,2012-12-06 Recently there has been increased interest in the development of computer aided design programs to support the system level designer of integrated circuits more actively Such design tools hold the promise of raising the level of abstraction at which an integrated circuit is designed thus releasing the current designers from many of the details of logic and circuit level design The promise further suggests that a whole new group of designers in neighboring engineering and science disciplines with far less understanding of integrated circuit design will also be able to increase their productivity and the functionality of the systems they design This promise has been made repeatedly as each new higher level of computer aided design tool is introduced and has repeatedly fallen short of fulfillment This book presents the results of research aimed at introducing yet higher levels of design tools that will inch the integrated circuit design community closer to the fulfillment of that promise 1 1 SYNTHESIS OF INTEGRATED CmCUITS In the integrated circuit Ie design process a behavior that meets certain specifications is conceived for a system the behavior is used to produce a design in terms of a set of structural logic elements and these logic elements are mapped onto physical units The design process is impacted by a set of constraints as well as technological information i e the logic elements and physical units used for the design **The MIPS-X RISC Microprocessor** Paul Chow,2013-03-09 The first Stanford MIPS project started as a special graduate course in 1981 That project produced working silicon in 1983 and a prototype for running small programs in early 1984 After that we declared it a success and decided to move on to the next project MIPS X This book is the final and complete word on MIPS X The initial design of MIPS X was formulated in 1984 beginning in the Spring At that time we were unsure that RISe technology was going to have the industrial impact that we felt it should We also knew of a number of architectural and implementation flaws in the Stanford MIPS machine We believed that a new processor could achieve a performance level of over 10 times a VAX 11 780 and that a microprocessor of this performance level would convince academic skeptics of the value of the RISe approach We were concerned that the flaws in the original RISe design might overshadow the core ideas or that attempts to industrialize the technology would repeat the mistakes of the first generation designs MIPS X was targeted to eliminate the flaws in the first generation de signs and to boost the performance level by over a factor of five **BiCMOS Technology and Applications** Antonio R. Alvarez,2013-03-09 The topic

of bipolar compatible CMOS BiCMOS is a fascinating one and of ever growing practical importance The technology pendulum has swung from the two extremes of preeminence of bipolar in the 1950s and 60s to the apparent endless horizons for VLSI NMOS technology during the 1970s and 80s Yet starting in the 1980s severallimits were clouding the horizon for pure NMOS technology CMOS reemerged as a viable high density high performance technology Similarly by the mid 1980s scaled bipolar devices had not only demonstrated new high speed records but early versions of mixed bipolar CMOS technology were being produced Hence the paradigm of either high density Q high speed was metamorphasizing into an opportunity for both speed and density via a BiCMOS approach Now as we approach the 1990s there have been a number of practical demonstrations of BiCMOS both for memory and logic applications and I expect the trend to escalate over the next decade This book makes a timely contribution to the field of BiCMOS technology and circuit development The evolution is now indeed rapid so that it is difficult to make such a book exhaustive of current developments Probably equally difficult is the fact that the new technology opens a range of novel circuit opportunities that are as yet only formative in their development Given these obstacles it is a herculean task to try to assemble a book on BiCMOS

Adopting the Track of Phrase: An Mental Symphony within **Switchlevel Timing Simulation Of Mos Vlsi Circuits**

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