Testability Concepts for Digital ICs
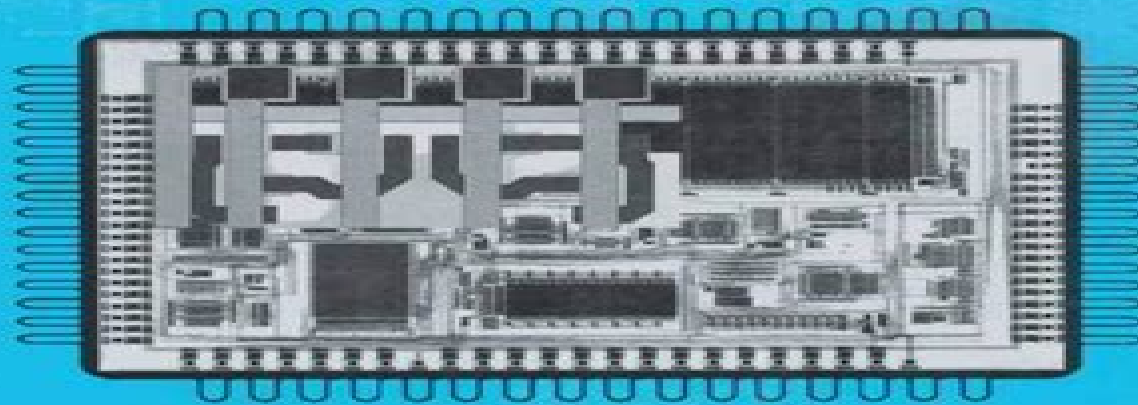
The Macro Test Approach

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Yervant Zorian

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　　Testability Concepts for Digital ICs F.P.M. Beenker,R.G. Bennetts,A.P. Thijssen,2012-12-06 Preface Testing Integrated Circuits for manufacturing defects includes four basic disciplines First of all an understanding of the origin and behaviour of defects Secondly knowledge of IC design and IC design styles Thirdly knowledge of how to create a test program for an IC which is targeted on detecting these defects and finally understanding of the hardware Automatic Test Equipment to run the test on All four items have to be treated managed and to a great extent integrated before the term IC quality gets a certain meaning and a test a certain measurable value The contents of this book reflects our activities on testability concepts for complex digital ICs as performed at Philips Research Laboratories in Eindhoven The Netherlands Based on the statements above we have worked along a long term plan which was based on four pillars 1 The definition of a test methodology suitable for future IC design styles 2 capable of handling improved defect models 3 supported by software tools and 4 providing an easy link to Automatic Test Equipment The reasoning we have followed was continuously focused on IC qUality Quality expressed in terms of the ability of delivering a customer a device with no residual manufacturing defects Bad devices should not escape a test The basis of IC quality is a thorough understanding of defects and defect models *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* M. Bushnell,Vishwani Agrawal,2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty,2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is

especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing   *Principles of Testing Electronic Systems* Samiha Mourad,Yervant Zorian,2000-07-25 A pragmatic approach to testing electronic systems As we move ahead in the electronic age rapid changes in technology pose an ever increasing number of challenges in testing electronic products Many practicing engineers are involved in this arena but few have a chance to study the field in a systematic way learning takes place on the job By covering the fundamental disciplines in detail Principles of Testing Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today s very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references   **Multi-Chip Module Test Strategies** Yervant Zorian,2012-12-06 MCMs today consist of complex and dense VLSI devices mounted into packages that allow little physical access to internal nodes The complexity and cost associated with their test and diagnosis are major obstacles to their use Multi Chip Module Test Strategies presents state of the art test strategies for MCMs This volume of original research is designed for engineers interested in practical implementations of MCM test solutions and for designers looking for leading edge test and design for testability solutions for their next designs Multi Chip Module Test Strategies consists of eight contributions by leading researchers It is designed to provide a comprehensive and well balanced coverage of the MCM test domain Multi Chip Module Test Strategies has also been published as a special issue of the Journal of Electronic Testing Theory and Applications JETTA Volume 10 Numbers 1 and 2   **Defect Oriented Testing for CMOS Analog and Digital Circuits** Manoj Sachdev,2013-06-29 Defect oriented testing is expected to play a significant role in coming generations of technology Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches Furthermore with increased level of integration an IC may contain diverse building blocks Such blocks include digital logic PLAs volatile and non volatile memories and analog interfaces For such diverse building blocks traditional fault modeling and test approaches will become increasingly inadequate Defect oriented testing methods have

come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits ICs have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject It is essential reading for all design and test professionals as well as researchers and students working in the field A strength of this book is its breadth Types of designs considered include analog and digital circuits programmable logic arrays and memories Having a fault model does not automatically provide a test Sometimes design for testability hardware is necessary Many design for testability ideas supported by experimental evidence are included from the Foreword by Vishwani D Agrawal *System-on-Chip Test Architectures* Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students *A Designer's Guide to Built-In Self-Test* Charles E. Stroud,2005-12-27 A recent technological advance is the art of designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer s perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations **The Computer Engineering Handbook** Vojin G. Oklobdzija,2001-12-26 There is arguably no field in greater need of a comprehensive handbook than computer engineering The unparalleled rate of technological advancement the explosion of computer applications and the now in progress migration to a wireless world

have made it difficult for engineers to keep up with all the developments in specialties outside their own References published only a few years ago are now sorely out of date The Computer Engineering Handbook changes all of that Under the leadership of Vojin Oklobdzija and a stellar editorial board some of the industry s foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering Instead of focusing on basic introductory material it forms a comprehensive state of the art review of the field s most recent achievements outstanding issues and future directions The world of computer engineering is vast and evolving so rapidly that what is cutting edge today may be obsolete in a few months While exploring the new developments trends and future directions of the field The Computer Engineering Handbook captures what is fundamental and of lasting value *Embedded Systems Handbook* Richard Zurawski,2005-08-16 Embedded systems are nearly ubiquitous and books on individual topics or components of embedded systems are equally abundant Unfortunately for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink Until now The Embedded Systems Handbook is an oasis of information offering a mix of basic a Research Perspectives and Case Studies in System Test and Diagnosis John W. Sheppard,William R. Simpson,2012-12-06 System level testing is becoming increasingly important It is driven by the incessant march of complexity which is forcing us to renew our thinking on the processes and procedures that we apply to test and diagnosis of systems In fact the complexity defines the system itself which for our purposes is any aggregation of related elements that together form an entity of sufficient complexity for which it is impractical to treat all of the elements at the lowest level of detail System approaches embody the partitioning of problems into smaller inter related subsystems that will be solved together Thus words like hierarchical dependence inference model and partitioning are frequent throughout this text Each of the authors deals with the complexity issue in a similar fashion but the real value in a collected work such as this is in the subtle differences that may lead to synthesized approaches that allow even more progress The works included in this volume are an outgrowth of the 2nd International Workshop on System Test and Diagnosis held in Alexandria Virginia in April 1998 The first such workshop was held in Freiburg Germany six years earlier In the current workshop nearly 50 experts from around the world struggled over issues concerning the subject In this volume a select group of workshop participants was invited to provide a chapter that expanded their workshop presentations and incorporated their workshop interactions While we have attempted to present the work as one volume and requested some revision to the work the content of the individual chapters was not edited significantly Consequently you will see different approaches to solving the same problems and occasional disagreement between authors as to definitions or the importance of factors The works collected in this volume represent the state of the art in system test and diagnosis and the authors are at the leading edge ofthat science From the Preface **Delay Fault Testing for VLSI Circuits** Angela Krstic,Kwang-Ting (Tim) Cheng,2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal

sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader s understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest **On-Line Testing for VLSI** Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Boundary-Scan Interconnect Diagnosis** José T. de Sousa,Peter Y.K. Cheung,2005-12-28 Boundary Scan Interconnect Diagnosis explains how to synthesize digital diagnostic sequences for wire interconnects using boundary scan and how to assess the quality of those sequences Its importance has to do with designing complex electronic systems using pre designed intellectual property IP cores which is becoming increasingly popular nowadays Since tests for pre designed cores can be supplied with the cores themselves the only additional tests that need to be developed to test and diagnose the entire system are those for wire interconnects between the cores Besides the trivial solutions that are often used to solve this problem there are many more methods that enable significant optimizations of test vector length and or diagnostic resolution The book surveys all existing methods of this kind and proposes new ones In the new approach circuit and interconnect faults are carefully modeled and graph techniques are applied to solve the problem The original feature of the new method is the fact that it can be adjusted to provide shorter test sequences and or greater diagnostic resolution The

effectiveness of existing and proposed methods is then evaluated using real electronic assemblies and published statistical data for an actual manufacturing process from HP *The Small Book About Design-for-Test* Juergen Alt,2025-05-30 This book is designed for individuals working in the semiconductor industry who need a fundamental understanding of Design for Test DfT methods It caters to test and product engineers who typically utilize these methods as well as chip designers project managers and business owners who seek to comprehend the value of implemented DfT methods Additionally it serves as a starting point for beginners in DfT before delving deeper into implementation tools and test pattern generation tasks Originating from a university lecture the core content of this book has expanded over the years It bridges the gap between theoretical textbook descriptions of DfT and its practical application in the industry The goal is to present DfT as a collection of methods that maintain manufacturing test costs at a level that allows for reasonable selling prices even for complex products utilizing the latest silicon technologies The book is structured into three parts The first part provides a summary of DfT techniques and an introduction to pattern generation techniques The second part delves into established DfT techniques for special analogmixed signal circuits and memories within the industry The third part proposes a systematic approach to test concept engineering maximizing the benefits of DfT methodologies By exploring the fundamentals and advanced concepts of DfT this book aims to equip readers with the knowledge and tools necessary to contribute to the ongoing innovation in semiconductor testing and development **Introduction to Advanced System-on-Chip Test Design and Optimization** Erik Larsson,2006-03-30 SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process **Introduction to IDDQ Testing** S. Chakravarty,Paul J. Thadikaran,2012-12-06 Testing techniques for VLSI circuits are undergoing many exciting changes The predominant method for testing digital circuits consists of applying a set of input stimuli to the IC and monitoring the logic levels at primary outputs If for one or more inputs there is a discrepancy between the observed output and the expected output then the IC is declared to be defective A new approach to testing digital circuits which has come to be known as IDDQ testing has been actively researched for the last fifteen years In IDDQ testing the steady state supply current rather than the logic levels at the primary outputs is monitored Years of research suggests that IDDQ testing can significantly improve the quality and reliability of fabricated circuits This has

prompted many semiconductor manufacturers to adopt this testing technique among them Philips Semiconductors Ford Microelectronics Intel Texas Instruments LSI Logic Hewlett Packard SUN microsystems Alcatel and SGS Thomson This increase in the use of IDDQ testing should be of interest to three groups of individuals associated with the IC business Product Managers and Test Engineers CAD Tool Vendors and Circuit Designers Introduction to IDDQ Testing is designed to educate this community The authors have summarized in one volume the main findings of more than fifteen years of research in this area   Formal Equivalence Checking and Design Debugging Shi-Yu Huang,Kwang-Ting (Tim) Cheng,2012-12-06 Formal Equivalence Checking and Design Debugging covers two major topics in design verification logic equivalence checking and design debugging The first part of the book reviews the design problems that require logic equivalence checking and describes the underlying technologies that are used to solve them Some novel approaches to the problems of verifying design revisions after intensive sequential transformations such as retiming are described in detail The second part of the book gives a thorough survey of previous and recent literature on design error diagnosis and design error correction This part also provides an in depth analysis of the algorithms used in two logic debugging software programs ErrorTracer and AutoFix developed by the authors From the Foreword With the adoption of the static sign off approach to verifying circuit implementations the application specific integrated circuit ASIC industry will experience the first radical methodological revolution since the adoption of logic synthesis Equivalence checking is one of the two critical elements of this methodological revolution This book is timely for either the designer seeking to better understand the mechanics of equivalence checking or for the CAD researcher who wishes to investigate well motivated research problems such as equivalence checking of retimed designs or error diagnosis in sequential circuits Kurt Keutzer University of California Berkeley   Reasoning in Boolean Networks Wolfgang Kunz,Dominik Stoffel,2013-03-09 Reasoning in Boolean Networks provides a detailed treatment of recent research advances in algorithmic techniques for logic synthesis test generation and formal verification of digital circuits The book presents the central idea of approaching design automation problems for logic level circuits by specific Boolean reasoning techniques While Boolean reasoning techniques have been a central element of two level circuit theory for many decades Reasoning in Boolean Networks describes a basic reasoning methodology for multi level circuits This leads to a unified view on two level and multi level logic synthesis The presented reasoning techniques are applied to various CAD problems to demonstrate their usefulness for today s industrially relevant problems Reasoning in Boolean Networks provides lucid descriptions of basic algorithmic concepts in automatic test pattern generation logic synthesis and verification and elaborates their intimate relationship to provide further intuition and insight into the subject Numerous examples are provide for ease in understanding the material Reasoning in Boolean Networks is intended for researchers in logic synthesis VLSI testing and formal verification as well as for integrated circuit designers who want to enhance their understanding of basic CAD methodologies   **System-on-Chip** Bashir M. Al-Hashimi,2006-01-31 This book

highlights both the key achievements of electronic systems design targeting SoC implementation style and the future challenges presented by the continuing scaling of CMOS technology

Ignite the flame of optimism with Get Inspired by is motivational masterpiece, **Testability Concepts For Digital Ics The Macro Test Approach** . In a downloadable PDF format (PDF Size: *), this ebook is a beacon of encouragement. Download now and let the words propel you towards a brighter, more motivated tomorrow.

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