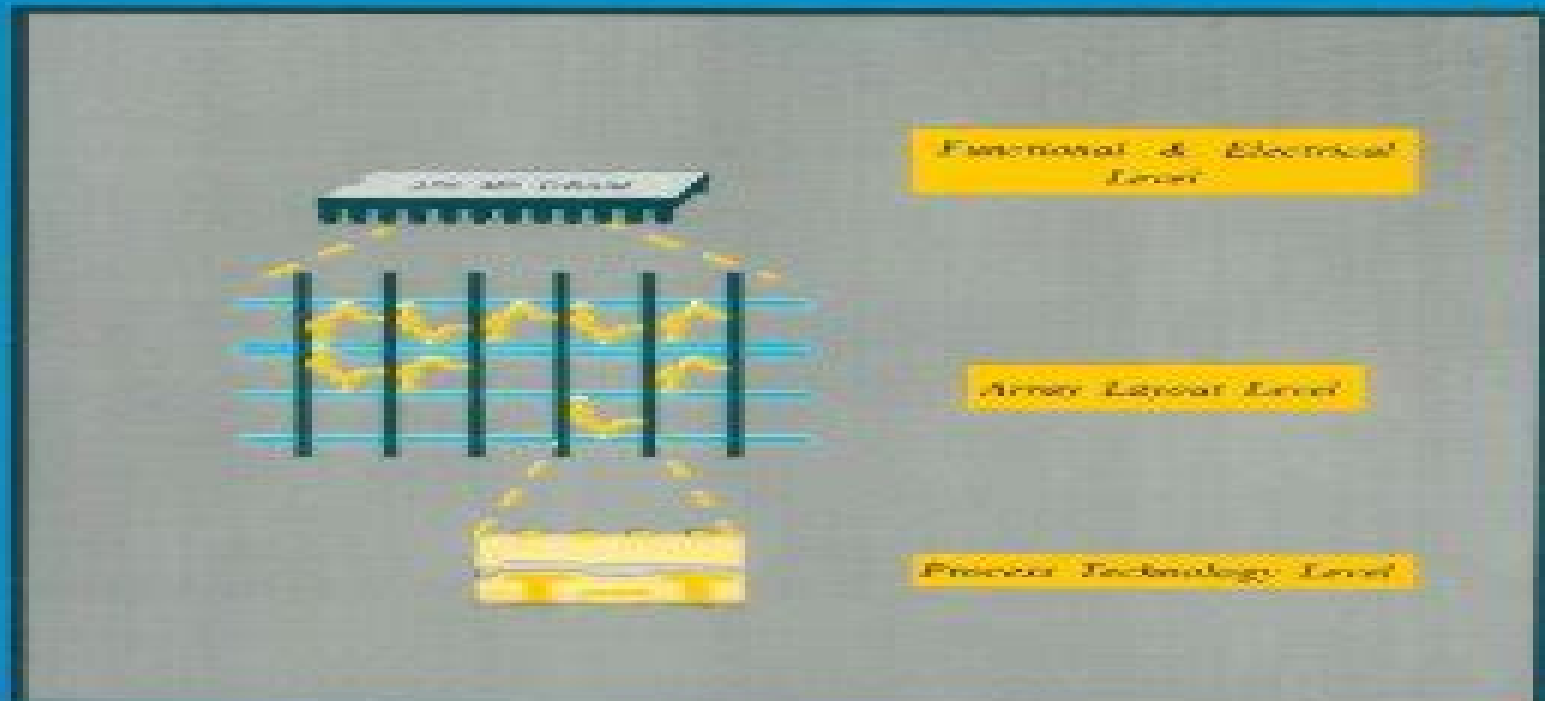


# TESTING AND TESTABLE DESIGN OF HIGH-DENSITY RANDOM-ACCESS MEMORIES

PINAKI MAZUMDER  
KANAD CHAKRABORTY



# Testing And Testable Design Of High Density Random Access Memories

**Angela Krstic, Kwang-Ting (Tim) Cheng**



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**Testing and Testable Design of High-Density Random-Access Memories** Pinaki Mazumder, Kanad Chakraborty, 1996-09-30 It is not in the interest of business leaders to turn public schools into vocational schools We can teach students how to be marketing people We can teach them how to manage balance sheets stated Louis V Gerstner Jr of IBM at the recent Education Summit meeting in New York He continued What is killing us is having to teach them to read and to compute and to communicate and to think TIME April 8 1996 page 40 The last sentence is most significant because it sets requirements for education and hence gives the specification for a textbook The textbook should contain all the necessary scientific information that the reader will need to practice the art in the technological world In addition to the scientific detail illustrative examples are necessary The book should teach science without restricting creativity and it should prepare the student for solving problems never encountered before In pursuing our goal of advancing the frontiers of test technology we must cover applications education and research This is the first textbook in the Frontiers series Semiconductor memories represent the frontier of VLSI in more ways than one First memories have always used more aggressive physical design rules and higher densities than other VLSI chips thus advancing the semiconductor technology Second the availability of low cost memory chips makes numerous software applications possible by fueling the demand for all types of chips

**Testing Static Random Access Memories** Said Hamdioui, 2013-06-29 Testing Static Random Access Memories covers testing of one of the important semiconductor memories types it addresses testing of static random access memories SRAMs both single port and multi port It contributes to the technical knowledge needed by those involved in memory testing engineers and researchers The book begins with outlining the most popular SRAMs architectures Then the description of realistic fault models based on defect injection and SPICE simulation are introduced Thereafter high quality and low cost test patterns as well as test strategies for single port two port and any p port SRAMs are presented together with some preliminary test results showing the importance of the new tests in reducing DPM level The impact of the port restrictions e g read only ports on the fault models tests and test strategies is also discussed Features Fault primitive based analysis of memory faults A complete framework of and classification memory faults A systematic way to develop optimal and high quality memory test algorithms A systematic way to develop test patterns for any multi port SRAM Challenges and trends in embedded memory testing

**High Performance Memory Testing** R. Dean Adams, 2005-12-29 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author's 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self

Test is written for the professional and the researcher to help them understand the memories that are being tested

Fault-tolerance and Reliability Techniques for High-density Random-access Memories Kanad Chakraborty, Pinaki Mazumder, 2002 This book deals with primarily with reliable and fault tolerant circuit design and evaluation techniques for RAMS It examines both the manufacturing fault tolerance e.g. self repair at the time of manufacturing and online and field related fault tolerance e.g. error correction It talks a lot about important techniques and requirements and explains what needs to be done and why for each of the techniques

**Design for AT-Speed Test, Diagnosis and Measurement** Benoit Nadeau-Dostie, 2006-04-11 Design for AT Speed Test Diagnosis and Measurement is the first book to offer practical and proven design for testability DFT solutions to chip and system design engineers test engineers and product managers at the silicon level as well as at the board and systems levels Designers will see how the implementation of embedded test enables simplification of silicon debug and system bring up Test engineers will determine how embedded test provides a superior level of at speed test diagnosis and measurement without exceeding the capabilities of their equipment Product managers will learn how the time resources and costs associated with test development manufacture cost and lifecycle maintenance of their products can be significantly reduced by designing embedded test in the product A complete design flow and analysis of the impact of embedded test on a design makes this book a must read before any DFT is attempted

*Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device technology circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signal subsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

On-Line Testing for VLSI Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope

on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers

**Delay Fault Testing for VLSI Circuits** Angela Krstic, Kwang-Ting (Tim) Cheng, 2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader's understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Techniques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest

*Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation* Alfredo Benso, Paolo Prinetto, 2005-12-15 Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation intends to be a comprehensive guide to Fault Injection techniques used to evaluate the dependability of a digital system The description and the critical analysis of different Fault Injection techniques and tools will be authored by key scientists in the field of system dependability and fault tolerance

*Power-Constrained Testing of VLSI Circuits* Nicola Nicolici, Bashir M. Al-Hashimi, 2006-04-11 This text focuses on techniques for minimizing power dissipation during test application at logic and register transfer levels of abstraction of the VLSI design flow It surveys existing techniques and presents several test automation techniques for reducing power in scan based sequential circuits and BIST data paths

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