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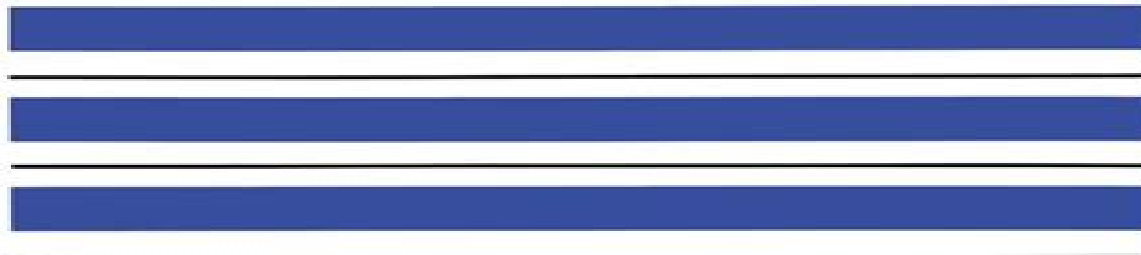
Monica S. Lam

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Systolic Array Optimizing Compiler

Monica S. Lam

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A Systolic Array Optimizing Compiler Monica S. Lam,2012-12-06 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high peiformance programmable systolic arrays represents a practical cost effective solu tion to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors   A Systolic Array Optimizing Compiler Monica S. Lam,2011-10-17 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high peiformance programmable systolic arrays represents a practical cost effective solu tion to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors   **A Systolic Array Optimizing Compiler** M. S.-L. Lam,1987   **A Systolic Array Parallelizing Compiler** Ping-Sheng Tseng,1990-08-31 Widespread use

of parallel processing will become a reality only if the process of porting applications to parallel computers can be largely automated Usually it is straightforward for a user to determine how an application can be mapped onto a parallel machine however the actual development of parallel code if done by hand is typically difficult and time consuming Parallelizing compilers which can gen erate parallel code automatically are therefore a key technology for parallel processing In this book Ping Sheng Tseng describes a parallelizing compiler for systolic arrays called AL Although parallelizing compilers are quite common for shared memory parallel machines the AL compiler is one of the first working parallelizing compilers for distributed memory machines of which systolic arrays are a special case The AL compiler takes advantage of the fine grain and high bandwidth interprocessor communication capabilities in a systolic architecture to generate efficient parallel code xii Foreword While capable of handling an important class of applications AL is not intended to be a general purpose parallelizing compiler   A Systolic Array Parallelizing Compiler Ping-Sheng Tseng,2012-12-06 Widespread use of parallel processing will become a reality only if the process of porting applications to parallel computers can be largely automated Usually it is straightforward for a user to determine how an application can be mapped onto a parallel machine however the actual development of parallel code if done by hand is typically difficult and time consuming Parallelizing compilers which can gen erate parallel code automatically are therefore a key technology for parallel processing In this book Ping Sheng Tseng describes a parallelizing compiler for systolic arrays called AL Although parallelizing compilers are quite common for shared memory parallel machines the AL compiler is one of the first working parallelizing compilers for distributed memory machines of which systolic arrays are a special case The AL compiler takes advantage of the fine grain and high bandwidth interprocessor communication capabilities in a systolic architecture to generate efficient parallel code xii Foreword While capable of handling an important class of applications AL is not intended to be a general purpose parallelizing compiler

Parallel Computing Technologies Victor Malyshkin,1997-08-06 This book constitutes the refereed proceedings of the Fourth International Conference on Parallel Computing Technologies PaCT 97 held in Yaroslavl Russia in September 1997 The volume presents a total of 54 contributions 21 full papers 20 short papers 10 posters and three tutorials All papers were selected for inclusion in the proceedings from numerous submissions on the basis of three independent reviews The volume covers all current topics in parallel processing it is divided into sections on theory software hardware and architecture applications posters and tutorials   **Conference Record of the Fifteenth Annual ACM Symposium on Principles of Programming Languages** ,1988   *Embedded Software for SoC* Ahmed Amine Jerraya,Sungjoo Yoo,Norbert Wehn,Diederik Verkest,2005-12-30 This title covers all software related aspects of SoC design from embedded and application domain specific operating systems to system architecture for future SoC It will give embedded software designers invaluable insights into the constraints imposed by the use of embedded software in an SoC context   **Mathematical Foundations Of Parallel Computing** V V Voevodin,1992-03-24 Parallel implementation of algorithms involves many

difficult problems In particular among them are round off analysis the way to convert sequential programs and algorithms into the parallel mode the choice of appropriate or optimal computer architect and so on To solve these problems it is necessary to know very well the structure of algorithms This book deal with the mathematical mechanism that permits us to investigate structures of both sequential and parallel algorithms This mechanism allows us to recognize and explain the relations between different methods of constructing parallel algorithms the methods of analysing round off errors the methods of optimizing memory traffic the methods of working out the fastest implementation for a given parallel computer and other methods attending the joint investigation of algorithms and computers   The Interaction of Compilation Technology and Computer Architecture David J. Lilja,Peter L. Bird,2012-12-06 In brief summary the following results were presented in this work A linear time approach was developed to find register requirements for any specified CS schedule or filled MRT An algorithm was developed for finding register requirements for any kernel that has a dependence graph that is acyclic and has no data reuse on machines with depth independent instruction templates We presented an efficient method of estimating register requirements as a function of pipeline depth We developed a technique for efficiently finding bounds on register require ments as a function of pipeline depth Presented experimental data to verify these new techniques discussed some interesting design points for register file size on a number of different architectures REFERENCES 1 Robert P Colwell Robert P Nix John J O Donnell David B Papworth and Paul K Rodman A VLIW Architecture for a Trace Scheduling Com piler In Architectural Support for Programming Languages and Operating Systems pages 180 192 1982 2 C Eisenbeis W Jalby and A Lichnewsky Compile Time Optimization of Memory and Register Usage on the Cray 2 In Proceedings of the Second Workshop on Languages and Compilers Urbana l inois August 1989 3 C Eisenbeis William Jalby and Alain Lichnewsky Squeezing More CPU Performance Out of a Cray 2 by Vector Block Scheduling In Proceedings of Supercomputing 88 pages 237 246 1988 4 Michael J Flynn Very High Speed Computing Systems Proceedings of the IEEE 54 1901 1909 December 1966   *Application of CLP to instruction modulo scheduling for VLIW processors* Łukasz Domagała,2012   Instruction-Level Parallelism B.R. Rau,J.A. Fisher,2012-12-06 Instruction Level Parallelism presents a collection of papers that attempts to capture the most significant work that took place during the 1980s in the area of instruction level ILP parallel processing The papers in this book discuss both compiler techniques and actual implementation experience on very long instruction word VLIW and superscalar architectures   **Embedded Multiprocessors** Sundararajan Sriram,Shuvra S. Bhattacharyya,2018-10-03 Techniques for Optimizing Multiprocessor Implementations of Signal Processing Applications An indispensable component of the information age signal processing is embedded in a variety of consumer devices including cell phones and digital television as well as in communication infrastructure such as media servers and cellular base stations Multiple programmable processors along with custom hardware running in parallel are needed to achieve the computation throughput required of such applications Reviews important research in key areas related to the multiprocessor

implementation of multimedia systemsEmbedded Multiprocessors Scheduling and Synchronization Second Edition presents architectures and design methodologies for parallel systems in embedded digital signal processing DSP applications It discusses application modeling techniques for multimedia systems the incorporation of interprocessor communication costs into multiprocessor scheduling decisions and a modeling methodology the synchronization graph for multiprocessor system performance analysis The book also applies the synchronization graph model to develop hardware and software optimizations that can significantly reduce the interprocessor communication overhead of a given schedule Chronicles recent activity dealing with single chip multiprocessors and dataflow modelsThis edition updates the background material on existing embedded multiprocessors including single chip multiprocessors It also summarizes the new research on dataflow models for signal processing that has been carried out since the publication of the first edition Harness the power of multiprocessorsThis book explores the optimization of interprocessor communication and synchronization in embedded multiprocessor systems It shows you how to design multiprocessor computer systems that are streamlined for multimedia applications **Compiler Optimizations for Scalable Parallel Systems** Santosh Pande,2001-04-18 Scalable parallel systems or more generally distributed memory systems offer a challenging model of computing and pose fascinating problems regarding compiler optimization ranging from language design to run time systems Research in this area is foundational to many challenges from memory hierarchy optimizations to communication optimization This unique handbook like monograph assesses the state of the art in the area in a systematic and comprehensive way The 21 coherent chapters by leading researchers provide complete and competent coverage of all relevant aspects of compiler optimization for scalable parallel systems The book is divided into five parts on languages analysis communication optimizations code generation and run time systems This book will serve as a landmark source for education information and reference to students practitioners professionals and researchers interested in updating their knowledge about or active in parallel computing *Systolic Signal Processing Systems* E. Swartzlander,2020-10-28 This book is about systolic signal processing systems networks of signal processors with efficient data flow between the processors It is written for students engineers and managers who wish a concise introduction to the key concepts and future directions of systolic processor architectures **The MIPS-X RISC Microprocessor** Paul Chow,2013-03-09 The first Stanford MIPS project started as a special graduate course in 1981 That project produced working silicon in 1983 and a prototype for running small programs in early 1984 After that we declared it a success and decided to move on to the next project MIPS X This book is the final and complete word on MIPS X The initial design of MIPS X was formulated in 1984 beginning in the Spring At that time we were unsure that RISe technology was going to have the industrial impact that we felt it should We also knew of a number of architectural and implementation flaws in the Stanford MIPS machine We believed that a new processor could achieve a performance level of over 10 times a VAX 11 780 and that a microprocessor of this performance level would convince academic skeptics of the value of the RISe approach

We were concerned that the flaws in the original RISe design might overshadow the core ideas or that attempts to industrialize the technology would repeat the mistakes of the first generation designs MIPS X was targeted to eliminate the flaws in the first generation de signs and to boost the performance level by over a factor of five **Computational Electronics** Karl Hess,J.P. Leburton,U. Ravaioli,2013-03-14 Large computational resources are of ever increasing importance for the simulation of semiconductor processes devices and integrated circuits The Workshop on Computational Electronics was intended to be a forum for the dis cussion of the state of the art of device simulation Three major research areas were covered conventional simulations based on the drift diffusion and the hydrodynamic models Monte Carlo methods and other techniques for the solution of the Boltzmann transport equation and computational approaches to quantum transport which are relevant to novel devices based on quantum interference and resonant tunneling phenomena Our goal was to bring together researchers from various disciplines that contribute to the advancement of device simulation These include Computer Sci ence Electrical Engineering Applied Physics and Applied Mathematics The suc cess of this multidisciplinary formula was proven by numerous interactions which took place at the Workshop and during the following three day Short Course on Computational Electronics The format of the course including a number of tutorial lectures and the large attendance of graduate students stimulated many discussions and has proven to us once more the importance of cross fertilization between the different disciplines **Principles of VLSI System Planning** Allen M. Dewey,Stephen W. Director,2012-12-06 This book describes a new type of computer aided VLSI design tool called a VLSI System Planning that is meant to aid designers dur ing the early or conceptual state of design During this stage of design the objective is to define a general design plan or approach that is likely to result in an efficient implementation satisfying the initial specifications or to determine that the initial specifications are not realizable A design plan is a collection of high level design decisions As an example the conceptual design of digital filters involves choosing the type of algorithm to implement e g finite impulse response or infinite impulse response the type of polyno mial approximation e g Equiripple or Chebyshev the fabrication technology e g CMOS or BiCMOS and so on Once a particu lar design plan is chosen the detailed design phase can begin It is during this phase that various synthesis simulation layout and test activities occur to refine the conceptual design gradually filling more detail until the design is finally realized The principal advantage of VLSI System Planning is that the increasingly expensive resources of the detailed design process are more efficiently managed Costly redesigns are minimized because the detailed design process is guided by a more credible consistent and correct design plan *Mixed-Mode Simulation* Resve A. Saleh,A. Richard Newton,2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily

available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques described in this book and so it can also serve as docu mentation for these programs ACKNOWLEDGEMENTS The authors would like to dedicate this book to Prof D O Peder son for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discus sions and collaborations with Jim Kleckner Young Kim Alberto Sangiovanni Vincentelli and Jacob White and we thank them for their contributions We also thank the countless others who participated in the research work and read early versions of this book Lillian Beck provided many useful suggestions to improve the manuscript Yun cheng Ju did the artwork for the illustrations   Wafer-Level Integrated Systems Stuart K. Tewksbury,2012-12-06 From the perspective of complex systems conventional Ie s can be regarded as discrete devices interconnected according to system design objectives imposed at the circuit board level and higher levels in the system implementation hierarchy However silicon monolithic circuits have progressed to such complex functions that a transition from a philosophy of integrated circuits Ie s to one of integrated sys tems is necessary Wafer scale integration has played an important role over the past few years in highlighting the system level issues which will most significantly impact the implementation of complex monolithic systems and system components Rather than being a revolutionary approach wafer scale integration will evolve naturally from VLSI as defect avoidance fault tolerance and testing are introduced into VLSI circuits Successful introduction of defect avoidance for example relaxes limits imposed by yield and cost on Ie dimensions allowing the monolithic circuit s area to be chosen according to the natural partitioning of a system into individual functions rather than imposing area limits due to defect densities The term wafer level is perhaps more appropriate than wafer scale A wafer level monolithic system component may have dimensions ranging from conventional yield limited Ie dimensions to full wafer dimensions In this sense wafer scale merely represents the obvious upper practical limit imposed by wafer sizes on the area of monolithic circuits The transition to monolithic wafer level integrated systems will require a mapping of the full range of system design issues onto the design of monolithic circuit

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