

System Synthesis with VHDL

Petru Eles, Krzysztof Kuchcinski and Zebo Peng

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System Synthesis With Vhdl A Transformational Approach

Abdoulaye Gamatié



System Synthesis With Vhdl A Transformational Approach:

System Synthesis with VHDL Petru Eles, Krzysztof Kuchcinski, Zebo Peng, 2013-03-14 Embedded systems are usually composed of several interacting components such as custom or application specific processors ASICs memory blocks and the associated communication infrastructure The development of tools to support the design of such systems requires a further step from high level synthesis towards a higher abstraction level The lack of design tools accepting a system level specification of a complete system which may include both hardware and software components is one of the major bottlenecks in the design of embedded systems Thus more and more research efforts have been spent on issues related to system level synthesis This book addresses the two most active research areas of design automation today high level synthesis and system level synthesis In particular a transformational approach to synthesis from VHDL specifications is described System Synthesis with VHDL provides a coherent view of system synthesis which includes the high level and the system level synthesis tasks VHDL is used as a specification language and several issues concerning the use of VHDL for high level and system level synthesis are discussed These include aspects from the compilation of VHDL into an internal design representation to the synthesis of systems specified as interacting VHDL processes The book emphasizes the use of a transformational approach to system synthesis A Petri net based design representation is rigorously defined and used throughout the book as a basic vehicle for illustration of transformations and other design concepts Iterative improvement heuristics such as tabu search simulated annealing and genetic algorithms are discussed and illustrated as strategies which are used to guide the optimization process in a transformation based design environment Advanced topics including hardware software partitioning test synthesis and low power synthesis are discussed from the perspective of a transformational approach to system synthesis System Synthesis with VHDL can be used for advanced undergraduate or graduate courses in the area of design automation and more specifically of high level and system level synthesis At the same time the book is intended for CAD developers and researchers as well as industrial designers of digital systems who are interested in new algorithms and techniques supporting modern design tools and methodologies System Synthesis with VHDL Petru Eles, Krzysztof Kuchcinski, Zebo Peng, 2014-01-15

Logic and Architecture Synthesis Gabriele Saucier, Anne Mignotte, 2016-01-09 This book describes several methods and systems solving one of the highlighted problems within computer aided design namely architectural and logic synthesis The book emphasises the most recent technologies in high level synthesis concentrating on applicative studies and practical constraints or criteria during synthesis Logic and Architecture Synthesis concentrates on the practical problems involving automatic synthesis of designs It is essential reading for researchers and CAD Managers working in this area

System-on-Chip Methodologies & Design Languages Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including

design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field EDA for IC System Design, Verification, and Testing Louis Scheffer, Luciano Lavagno, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set

Custom Memory Management Methodology Francky Catthoor, Sven Wuytack, G.E. de Greef, Florin Banica, Lode Nachtergaele, Arnout Vandecappelle, 2013-03-09 The main intention of this book is to give an impression of the state of the art in system level memory management data transfer and storage related issues for complex data dominated real time signal and data processing applications The material is based on research at IMEC in this area in the period 1989 1997 In order to deal with the stringent timing requirements and the data dominated characteristics of this domain we have adopted a target architecture style and a systematic methodology to make the exploration and optimization of such systems feasible Our approach is also very heavily application driven which is illustrated by several realistic demonstrators partly used as red thread examples in the book Moreover the book addresses only the steps above the traditional high level synthesis scheduling and allocation or compilation traditional or ILP oriented tasks The latter are mainly focussed on scalar or scalar stream operations and data where the internal structure of the complex data types is not exploited in contrast to the approaches discussed here The proposed methodologies are largely independent of the level of programmability in the data path and controller so they are valuable for the realisation of both hardware and software systems Our target domain consists of signal and data processing systems which deal with large amounts of data *Practical Formal Methods for Hardware Design* Carlos Delgado Kloos, Werner Damm, 2012-12-06 Formal methods for hardware design still find limited use in industry Yet current practice has to change to cope with decreasing design times and increasing quality requirements This research report presents results from the Esprit project FORMAT formal methods in hardware verification which involved the collaboration of the enterprises Siemens Italtel Telefonica I D TGI and AHL the research institute OFFIS and the universities of Madrid and Passau The work presented involves advanced specification languages for hardware design that are intuitive to the designer like timing diagrams and state based languages as well as their relation to VHDL and formal languages like temporal logic and a process algebraic calculus The results of experimental tests of the tools are also presented 6th IEEE International Workshop on Rapid System Prototyping Rudy Lauwereins, 1995 To help designers and developers of hardware

software systems knock together a working model more quickly the 33 papers discuss models for system simulation and emulation in a hierarchical sense software to hardware mapping software prototyping and validation prototyping environments of hardware Applications and Theory of Petri Nets 2004 Jordi Cortadella,Wolfgang Reisig,2004-06-15 This book constitutes the refereed proceedings of the 25th International Conference on Applications and Theory of Petri Nets ICATPN 2004 held in Bologna Italy in June 2004 The 19 revised full regular papers and 5 revised tool presentation papers presented together with 6 invited papers were carefully reviewed and selected from 62 submissions All current issues on research and development in the area of Petri nets are addressed in particular concurrent systems design and analysis modular systems development formal specification model validation model checking workflow management flow charts networking formal methods in software engineering etc **Formal Description Techniques and Protocol Specification, Testing and Verification** Stan Budkowski,Ana Cavalli,Elie Najm,2013-04-17 Formal Description Techniques and Protocol Specification Testing and Verification addresses formal description techniques FDTs applicable to distributed systems and communication protocols It aims to present the state of the art in theory application tools and industrialization of FDTs Among the important features presented are FDT based system and protocol engineering FDT application to distributed systems Protocol engineering Practical experience and case studies Formal Description Techniques and Protocol Specification Testing and Verification comprises the proceedings of the Joint International Conference on Formal Description Techniques for Distributed Systems and Communication Protocols and Protocol Specification Testing and Verification sponsored by the International Federation for Information Processing held in November 1998 Paris France Formal Description Techniques and Protocol Specification Testing and Verification is suitable as a secondary text for a graduate level course on Distributed Systems or Communications and as a reference for researchers and practitioners in industry

Computing in Research and Development in Africa Abdoulaye Gamatié,2014-10-11 This book describes the trends challenges and solutions in computing use for scientific research and development within different domains in Africa such as health agriculture environment economy energy education and engineering The benefits expected are discussed by a number of recognized domain specific experts with a common theme being computing as solution enabler This book is the first document providing such a representative up to date view on this topic at the continent level *Distributed, Parallel and Biologically Inspired Systems* Mike Hinchey,Bernd Kleinjohann,Lisa Kleinjohann,Peter Lindsay,Franz J. Rammig,Jon Timmis,Marilyn Wolf,2010-08-06 st This volume contains the proceedings of two conferences held as part of the 21 IFIP World Computer Congress in Brisbane Australia 20 23 September 2010 th The first part of the book presents the proceedings of DIPES 2010 the 7 IFIP Conference on Distributed and Parallel Embedded Systems The conference introduced in a separate preface by the Chairs covers a range of topics from specification and design of embedded systems through to dependability and fault tolerance rd The second part of the book contains the proceedings of BICC 2010 the 3 IFIP Conference on

Biologically Inspired Collaborative Computing The conference is concerned with emerging techniques from research areas such as organic computing autonomic computing and self adaptive systems where inspiration for techniques comes from exhibited behaviour in nature and biology Such techniques require the use of research developed by the DIPES community in supporting collaboration over multiple systems We hope that the combination of the two proceedings will add value for the reader and advance our related work Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference 1997, January 28-31, 1997, Makuhari Messe, Nippon Convention Center, Chiba, Japan IEEE Circuits and Systems Society, 1996 The Asia and South Pacific conference on design automation is the second in a series of biennial international conferences It aims to provide the CAD DA community with the opportunity to present ideas and concepts on upstream design as well as methodologies of downstream design Design Methods and Applications for Distributed Embedded Systems Bernd Kleinjohann, Guang R. Gao, Hermann Kopetz, Lisa Kleinjohann, Achim Rettberg, 2004-07-27 The IFIP TC 10 Working Conference on Distributed and Parallel Embedded Systems DIPES 2004 brings together experts from industry and academia to discuss recent developments in this important and growing field in the splendid city of Toulouse France The ever decreasing price performance ratio of microcontrollers makes it economically attractive to replace more and more conventional mechanical or electronic control systems within many products by embedded real time computer systems An embedded real time computer system is always part of a well specified larger system which we call an intelligent product Although most intelligent products start out as stand alone units many of them are required to interact with other systems at a later stage At present many industries are in the middle of this transition from stand alone products to networked embedded systems This transition requires reflection and architecting The complexity of the evolving distributed artifact can only be controlled if careful planning and principled design methods replace the hoc engineering of the first version of many standalone embedded products *Design and Analysis of Distributed Embedded Systems* Bernd Kleinjohann, K.H. (Kane) Kim, Lisa Kleinjohann, Achim Rettberg, 2013-04-17 Design and Analysis of Distributed Embedded Systems is organized similar to the conference Chapters 1 and 2 deal with specification methods and their analysis while Chapter 6 concentrates on timing and performance analysis Chapter 3 describes approaches to system verification at different levels of abstraction Chapter 4 deals with fault tolerance and detection Middleware and software reuse aspects are treated in Chapter 5 Chapters 7 and 8 concentrate on the distribution related topics such as partitioning scheduling and communication The book closes with a chapter on design methods and frameworks **Masters Theses in the Pure and Applied Sciences** Wade H. Shafer, 2012-12-06 Masters Theses in the Pure and Applied Sciences was first conceived published and disseminated by the Center for Information and Numerical Data Analysis and Synthesis CINDAS at Purdue University in 1957 starting its coverage of theses with the academic year 1955 Beginning with Volume 13 the printing and dissemination phases of the activity were transferred to University Microfilms Xerox of Ann Arbor Michigan with the thought that such an arrangement

would be more beneficial to the academic and general scientific and technical community After five years of this joint undertaking we had concluded that it was in the interest of all concerned if the printing and distribution of the volumes were handled by an international publishing house to assure improved service and broader dissemination Hence starting with Volume 18 Masters Theses in the Pure and Applied Sciences has been disseminated on a worldwide basis by Plenum Publishing Corporation of New York and in the same year the coverage was broadened to include Canadian universities All back issues can also be ordered from Plenum We have reported in Volume 37 thesis year 1992 a total of 12 549 thesis titles from 25 Canadian and 153 United States universities We are sure that this broader base for these titles reported will greatly enhance the value of this important annual reference work While Volume 37 reports theses submitted in 1992 on occasion certain universities do report theses submitted in previous years but not reported at the time

High-Level Verification

Sudipta Kundu, Sorin Lerner, Rajesh K. Gupta, 2011-05-18 Given the growing size and heterogeneity of Systems on Chip SOC the design process from initial specification to chip fabrication has become increasingly complex This growing complexity provides incentive for designers to use high level languages such as C SystemC and SystemVerilog for system level design While a major goal of these high level languages is to enable verification at a higher level of abstraction allowing early exploration of system level designs the focus so far for validation purposes has been on traditional testing techniques such as random testing and scenario based testing This book focuses on high level verification presenting a design methodology that relies upon advances in synthesis techniques as well as on incremental refinement of the design process These refinements can be done manually or through elaboration tools This book discusses verification of specific properties in designs written using high level languages as well as checking that the refined implementations are equivalent to their high level specifications The novelty of each of these techniques is that they use a combination of formal techniques to do scalable verification of system designs completely automatically The verification techniques presented in this book include methods for verifying properties of high level designs and methods for verifying that the translation from high level design to a low level Register Transfer Language RTL design preserves semantics Used together these techniques guarantee that properties verified in the high level design are preserved through the translation to low level RTL

Computer Hardware

Description Languages and their Applications D. Borrione, R. Waxman, 2014-06-28 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

Readings in Hardware/Software Co-Design Giovanni De Micheli, Rolf Ernst, Wayne Wolf, 2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception

in the early 90s **FPGA-based Implementation of Signal Processing Systems** Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, 2008-10-13 Field programmable gate arrays FPGAs are an increasingly popular technology for implementing digital signal processing DSP systems By allowing designers to create circuit architectures developed for the specific applications high levels of performance can be achieved for many DSP applications providing considerable improvements over conventional microprocessor and dedicated DSP processor solutions The book addresses the key issue in this process specifically the methods and tools needed for the design optimization and implementation of DSP systems in programmable FPGA hardware It presents a review of the leading edge techniques in this field analyzing advanced DSP based design flows for both signal flow graph SFG based and dataflow based implementation system on chip SoC aspects and future trends and challenges for FPGAs The automation of the techniques for component architectural synthesis computational models and the reduction of energy consumption to help improve FPGA performance are given in detail Written from a system level design perspective and with a DSP focus the authors present many practical application examples of complex DSP implementation involving high performance computing e g matrix operations such as matrix multiplication high speed filtering including finite impulse response FIR filters and wave digital filters WDFs adaptive filtering e g recursive least squares RLS filtering transforms such as the fast Fourier transform FFT FPGA based Implementation of Signal Processing Systems is an important reference for practising engineers and researchers working on the design and development of DSP systems for radio telecommunication information audio visual and security applications Senior level electrical and computer engineering graduates taking courses in signal processing or digital signal processing shall also find this volume of interest

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