System Level Design of Reconfigurable Systems-on-Chip

Edited by
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Springer

System Level Design Of Reconfigurable Systems On Chips

Martin Radetzki

System Level Design Of Reconfigurable Systems On Chips:

System Level Design of Reconfigurable Systems-on-Chip Nikolaos Voros,Konstantinos Masselos,2006-02-23 System Level Design of Reconfigurable Systems on Chip provides insight in the challenges and difficulties encountered during the design of reconfigurable Systems on Chip SoCs Reconfiguration is becoming an important part of System on Chip design to cope with the increasing demands for simultaneous flexibility and computational power The book focuses on system level design issues for reconfigurable SoCs and provides information on reconfiguration aspects of complex SoCs and how they can be implemented in practice It is divided in three parts The first part provides background information and requirements on reconfigurable technologies and systems The second one identifies existing methodological gaps and introduces a design flow for developing reconfigurable Systems on Chip The high level part of the design flow can be covered by two C based methodologies one based on SystemC and one based on OCAPI XL both including appropriate extensions to handle reconfiguration issues Finally the third part of the book presents reconfigurable SoCs from the perspective of the designer through three indicative case studies from the wireless and multimedia communication domain   Dynamic System Reconfiguration in Heterogeneous Platforms Nikolaos Voros,Alberto Rosti,Michael Hübner,2009-05-28 Dynamic System Reconfiguration in Heterogeneous Platforms defines the MORPHEUS platform that can join the performance density advantage of reconfigurable technologies and the easy control capabilities of general purpose processors It consists of a System on Chip made of a scalable system infrastructure hosting heterogeneous reconfigurable accelerators providing dynamic reconfiguration capabilities and data stream management capabilities   **VLSI-SoC: Research Trends in VLSI and Systems on Chip** Giovanni De Micheli,Salvador Mir,Ricardo Reis,2010-08-23 This book contains extended and revised versions of the best papers presented during the fourteenth IFIP TC 10 WG 10 5 International Conference on Very Large Scale Integration This conference provides a forum to exchange ideas and show industrial and academic research results in microelectronics design The current trend toward increasing chip integration and technology process advancements brings about stimulating new challenges both at the physical and system design levels   *Languages for Embedded Systems and their Applications* Martin Radetzki,2009-05-24 Embedded systems take over complex control and data processing tasks in diverse application elds such as automotive avionics consumer products and telec munications They are the primary driver for improving overall system safety ef ciency and comfort The demand for further improvement in these aspects can only be satis ed by designing embedded systems of increasing complexity which in turn necessitates the development of new system design methodologies based on speci cation design and veri cation languages The objective of the book at hand is to provide researchers and designers with an overview of current research trends results and application experiences in c puter languages for embedded systems The book builds upon the most relevant contributions to the 2008 conference Forum on Design Languages FDL the p mier international conference specializing in this eld These contributions have been selected

based on the results of reviews provided by leading experts from search and industry In many cases the authors have improved their original work by adding breadth depth or explanation   Dynamically Reconfigurable Systems Marco Platzner,Norbert Wehn,2010-03-10 Dynamically Reconfigurable Systems is the first ever to focus on the emerging field of Dynamically Reconfigurable Computing Systems While programmable logic and design time configurability are well elaborated and covered by various texts this book presents a unique overview over the state of the art and recent results for dynamic and run time reconfigurable computing systems Reconfigurable hardware is not only of utmost importance for large manufacturers and vendors of microelectronic devices and systems but also a very attractive technology for smaller and medium sized companies Hence Dynamically Reconfigurable Systems also addresses researchers and engineers actively working in the field and provides them with information on the newest developments and trends in dynamic and run time reconfigurable systems   **Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication** Shen, Jih-Sheng,Hsiung, Pao-Ann,2010-06-30 Reconfigurable computing brings immense flexibility to on chip processing while network on chip has improved flexibility in on chip communication Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems on chip This book is the one of the first compilations written to demonstrate this future for network on chip design Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques to task assigning scheduling and arrival to designing an operating system to take advantage of the computing and communication flexibilities brought about by run time reconfiguration and network on chip it represents a complete source of the techniques and applications for reconfigurable network on chip necessary for understanding of future of this field   *System Level Design from HW/SW to Memory for Embedded Systems* Marcelo Götz,Gunar Schirner,Marco Aurélio Wehrmeister,Mohammad Abdullah Al Faruque,Achim Rettberg,2018-04-16 This book constitutes the refereed proceedings of the 5th IFIP TC 10 International Embedded Systems Symposium IESS 2015 held in Foz do Igua u Brazil in November 2015 The 18 full revised papers presented were carefully reviewed and selected from 25 submissions The papers present a broad discussion on the design analysis and verification of embedded and cyber physical systems including design methodologies verification performance analysis and real time systems design They are organized in the following topical sections cyber physical systems system level design multi many core system design memory system design and embedded HW SW design and applications   *Multiprocessor Systems-on-Chips* Ahmed Jerraya,Wayne Wolf,2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs Design topics include multiprocessor architectures

processors operating systems compilers methodologies and synthesis algorithms and application areas covered include telecommunications and multimedia The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs After having refined their material at the workshop the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology Examines several different architectures and the constraints imposed on them Discusses scheduling real time operating systems and compilers Analyzes design trade off and decisions in telecommunications and multimedia applications **Advances in VLSI and Embedded Systems** Anand D. Darji,Deepak Joshi,Amit Joshi,Ray Sheriff,2022-11-30 This book presents select peer reviewed proceedings of the 2nd International Conference on Advances in VLSI and Embedded Systems AVES 2021 This book covers cutting edge original research in VLSI design devices and emerging technologies embedded systems and CAD for VLSI To address the demand for complex and high functionality systems as well as portable consumer electronics the contents focus on advanced topics of circuit and systems design fabrication testing and standardization This book is useful for students researchers as well as industry professionals interested in emerging trends in VLSI and embedded systems **Advances in VLSI and Embedded Systems** Zuber Patel,Shilpi Gupta,Nithin Kumar Y. B.,2020-08-28 This book presents select peer reviewed proceedings of the International Conference on Advances in VLSI and Embedded Systems AVES 2019 held at SVNIT Surat Gujarat India The book covers cutting edge original research in VLSI design devices and emerging technologies embedded systems and CAD for VLSI With an aim to address the demand for complex and high functionality systems as well as portable consumer electronics the contents focus on basic concepts of circuit and systems design fabrication testing and standardization This book can be useful for students researchers as well as industry professionals interested in emerging trends in VLSI and embedded systems **Bio-Inspired Fault-Tolerant Algorithms for Network-on-Chip** Muhammad Athar Javed Sethi,2020-03-17 Network on Chip NoC addresses the communication requirement of different nodes on System on Chip The bio inspired algorithms improve the bandwidth utilization maximize the throughput and reduce the end to end latency and inter flit arrival time This book exclusively presents in depth information regarding bio inspired algorithms solving real world problems focussing on fault tolerant algorithms inspired by the biological brain and implemented on NoC It further documents the bio inspired algorithms in general and more specifically in the design of NoC It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters Key Features Covers bio inspired solutions pertaining to Network on Chip NoC design solving real world examples Includes bio inspired NoC fault tolerant algorithms with detail coding examples Lists fault tolerant algorithms with detailed examples Reviews basic concepts of NoC Discusses NoC architectures developed to date **Applied Reconfigurable Computing** Christian

Hochberger,Brent Nelson,Andreas Koch,Roger Woods,Pedro Diniz,2019-04-02 This book constitutes the proceedings of the 15th International Symposium on Applied Reconfigurable Computing ARC 2019 held in Darmstadt Germany in April 2019 The 20 full papers and 7 short papers presented in this volume were carefully reviewed and selected from 52 submissions In addition the volume contains 1 invited paper The papers were organized in topical sections named Applications partial reconfiguration and security image video processing high level synthesis CGRAs and vector processing architectures design frameworks and methodology convolutional neural networks   Parallel and Distributed Processing Jose Rolim,1998-03-18 This book constitutes the refereed proceedings of 10 international workshops held in conjunction with the merged 1998 IPPS SPDP symposia held in Orlando Florida US in March April 1998 The volume comprises 118 revised full papers presenting cutting edge research or work in progress In accordance with the workshops covered the papers are organized in topical sections on reconfigurable architectures run time systems for parallel programming biologically inspired solutions to parallel processing problems randomized parallel computing solving combinatorial optimization problems in parallel PC based networks of workstations fault tolerant parallel and distributed systems formal methods for parallel programming embedded HPC systems and applications and parallel and distributed real time systems   Field Programmable Logic and Application Jürgen Becker,Marco Platzner,Serge Vernalde,2004-08-19 This book constitutes the refereed proceedings of the 14th International Conference on Field Programmable Logic FPL 2003 held in Leuven Belgium in August September 2004 The 78 revised full papers 45 revised short papers and 29 poster abstracts presented together with 3 keynote contributions and 3 tutorial summaries were carefully reviewed and selected from 285 papers submitted The papers are organized in topical sections on organic and biologic computing security and cryptography platform based design algorithms and architectures acceleration application architecture physical design arithmetic multitasking circuit technology network processing testing applications signal processing computational models and compiler dynamic reconfiguration networks and optimisation algorithms system on chip high speed design image processing network on chip power aware design IP based design co processing architectures system level design physical interconnect computational models cryptography and compression network applications and architecture and debugging and test   **On-Chip Interconnect with aelite** Andreas Hansson,Kees Goossens,2010-10-20 The book provides a comprehensive description and implementation methodology for the Philips NXP Aethereal aelite Network on Chip NoC The presentation offers a systems perspective starting from the system requirements and deriving and describing the resulting hardware architectures embedded software and accompanying design flow Readers get an in depth view of the interconnect requirements not centered only on performance and scalability but also the multi faceted application driven requirements in particular composability and predictability The book shows how these qualitative requirements are implemented in a state of the art on chip interconnect and presents the realistic quantitative costs   Education for the 21st Century - Impact of ICT and Digital Resources Deepak Kumar,Joe

Turner,2006-10-11 It is a pleasure to offer you this book containing papers about ICT and education from the World Computer Congress 2006 WCC 2006 held in Santiago Chile and sponsored by the International Federation for Information Processing IFIP A lot of people worked very hard to make this event happen and to produce this book The programme committee with IFIP members from around the world issued a call for papers inspiring almost 80 people to submit papers posters demonstrations and workshops to the IFIP TC3 Technical Committee on Education sub conference of WCC 2006 The submitted papers were reviewed by a large group of referees to select the papers to be presented at the conference What is really amazing is that all these people freely contributed their time and effort to do all this work The TC3 sub conference of WCC 2006 has two themes Informatics Curricula TEaching Methods and best practice ICTEM II and Teaching and Learning with ICT Theory Policy and Practice These themes represent many of the broad range of interests of the Working Groups of IFIP TC3 Two kinds of papers are included in this book full papers and short papers Full papers are standard papers that are appropriate for an international conference on ICT and informatics education Of the 64 full paper submissions 28 44% were accepted A short paper represents work in progress opinion a proposal work with untested results or an experience report

Nature-Inspired Networking Phan Cong-Vinh,2018-02-13 Nature inspired includes roughly speaking bio inspired physical inspired social inspired and so on This book contains highly original contributions about how nature is going to shape networking systems of the future Hence it focuses on rigorous approaches and cutting edge solutions which encompass three classes of major methods 1 Those that take inspiration from nature for the development of novel problem solving techniques 2 Those that are based on the use of networks to synthesize natural phenomena and 3 Those that employ natural materials to compute or communicate **18th International Conference on Architecture of Computing Systems, ARCS 2005** Paul Lukowicz,2005 <u>Microelectrofluidic Systems</u> Tianhao Zhang,Krishnendu Chakrabarty,Richard B. Fair,2018-10-08 Composite systems that integrate microelectromechanical and microelectrofluidic MEF components with electronics are emerging as the next generation of system on a chip SOC designs However there remains a pressing need for a structured methodology for MEFS design automation including modeling techniques and simulation and optimization tools Integrating top down and bottom up design philosophies Microelectrofluidic Systems presents the first comprehensive design strategy for MEFS This strategy supports hierarchical modeling and simulation from the component level to the system level It leads to multi objective optimization tools valuable in all phases of the design process from conceptualization to final manufacturing The authors begin by defining the basic variables and elements needed to describe MEFS behavior then model that behavior across three layers of abstraction the low level component high level reconfigurable architecture and bio chemical application layers They have developed a hierarchical integrated design environment with SystemC and present its architecture and associated functional packages Microelectrofluidic Systems is visionary in its leverage of electronic design principles for microsystem design and heralds a new era of automated SOC design The strategy it presents holds the

potential for significant reductions in design time and life cycle maintenance costs and its techniques and tools for robust design and application flexibility can lead to the high volume production needed for the inevitably growing product market

Reconfigurable Computing Systems Engineering Lev Kirischian,2017-12-19 Reconfigurable Computing Systems Engineering Virtualization of Computing Architecture describes the organization of reconfigurable computing system RCS architecture and discusses the pros and cons of different RCS architecture implementations Providing a solid understanding of RCS technology and where it s most effective this book Details the architecture organization of RCS platforms for application specific workloads Covers the process of the architectural synthesis of hardware components for system on chip SoC for the RCS Explores the virtualization of RCS architecture from the system and on chip levels Presents methodologies for RCS architecture run time integration according to mode of operation and rapid adaptation to changes of multi parametric constraints Includes illustrative examples case studies homework problems and references to important literature A solutions manual is available with qualifying course adoption Reconfigurable Computing Systems Engineering Virtualization of Computing Architecture offers a complete road map to the synthesis of RCS architecture exposing hardware design engineers system architects and students specializing in designing FPGA based embedded systems to novel concepts in RCS architecture organization and virtualization

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