SYNTHESIS OF FINITE STATE MACHINES:
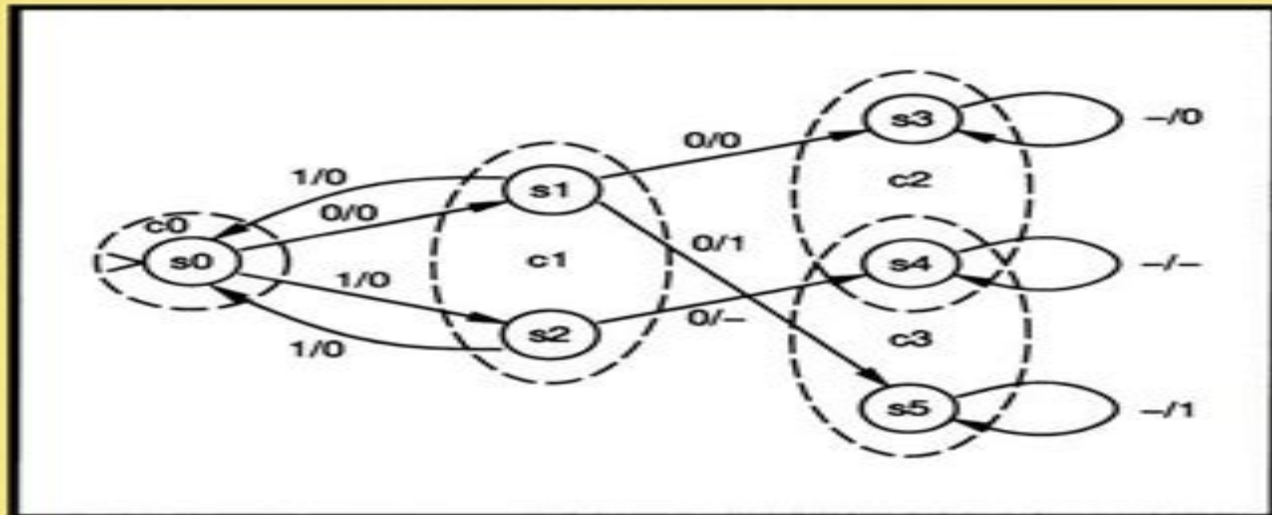## Functional Optimization

Timothy Kam
Tiziano Villa
Robert Brayton
Alberto Sangiovanni-Vincentelli

Synthesis Of Finite State Machines Functional Optimization

Alexander Barkalov,Larysa Titarenko,Jacek Bieganowski

Synthesis Of Finite State Machines Functional Optimization:

Synthesis of Finite State Machines Timothy Kam,Tiziano Villa,Robert K. Brayton,Alberto L. Sangiovanni-Vincentelli,2013-03-09 Synthesis of Finite State Machines Functional Optimization is one of two monographs devoted to the synthesis of Finite State Machines FSMs This volume addresses functional optimization whereas the second addresses logic optimization By functional optimization here we mean the body of techniques that compute all permissible sequential functions for a given topology of interconnected FSMs and select a best sequential function out of the permissible ones The result is a symbolic description of the FSM representing the chosen sequential function By logic optimization here we mean the steps that convert a symbolic description of an FSM into a hardware implementation with the goal to optimize objectives like area testability performance and so on Synthesis of Finite State Machines Functional Optimization is divided into three parts The first part presents some preliminary definitions theories and techniques related to the exploration of behaviors of FSMs The second part presents an implicit algorithm for exact state minimization of incompletely specified finite state machines ISFSMs and an exhaustive presentation of explicit and implicit algorithms for the binate covering problem The third part addresses the computation of permissible behaviors at a node of a network of FSMs and the related minimization problems of non deterministic finite state machines NDFSMs Key themes running through the book are the exploration of behaviors contained in a non deterministic FSM NDFSM and the representation of combinatorial problems arising in FSM synthesis by means of Binary Decision Diagrams BDDs Synthesis of Finite State Machines Functional Optimization will be of interest to researchers and designers in logic synthesis CAD and design automation **Synthesis of Finite State Machines** Timothy Kam,Tiziano Villa,Robert K. Brayton,2014-01-15 **Synthesis of Finite State Machines** Tiziano Villa,Timothy Kam,Robert K. Brayton,Alberto L. Sangiovanni-Vincentelli,2012-12-06 Synthesis of Finite State Machines Logic Optimization is the second in a set of two monographs devoted to the synthesis of Finite State Machines FSMs The first volume Synthesis of Finite State Machines Functional Optimization addresses functional optimization whereas this one addresses logic optimization The result of functional optimization is a symbolic description of an FSM which represents a sequential function chosen from a collection of permissible candidates Logic optimization is the body of techniques for converting a symbolic description of an FSM into a hardware implementation The mapping of a given symbolic representation into a two valued logic implementation is called state encoding or state assignment and it impacts heavily area speed testability and power consumption of the realized circuit The first part of the book introduces the relevant background presents results previously scattered in the literature on the computational complexity of encoding problems and surveys in depth old and new approaches to encoding in logic synthesis The second part of the book presents two main results about symbolic minimization a new procedure to find minimal two level symbolic covers under face dominance and disjunctive constraints and a unified frame to check encodability of encoding constraints and find codes of minimum length

that satisfy them The third part of the book introduces generalized prime implicants GPIs which are the counterpart in symbolic minimization of two level logic to prime implicants in two valued two level minimization GPIs enable the design of an exact procedure for two level symbolic minimization based on a covering step which is complicated by the need to guarantee encodability of the final cover A new efficient algorithm to verify encodability of a selected cover is presented If a cover is not encodable it is shown how to augment itminimally until an encodable superset of GPIs is determined To handle encodability the authors have extended the frame to satisfy encoding constraints presented in the second part The covering problems generated in the minimization of GPIs tend to be very large Recently large covering problems have been attacked successfully by representing the covering table with binary decision diagrams BDD In the fourth part of the book the authors introduce such techniques and extend them to the case of the implicit minimization of GPIs where the encodability and augmentation steps are also performed implicitly Synthesis of Finite State Machines Logic Optimization will be of interest to researchers and professional engineers who work in the area of computer aided design of integrated circuits **Synthesis of Finite State Machines** Tiziano Villa,Timothy Kam,Robert K Brayton,1997-04-01 Logic Synthesis for Finite State Machines Based on Linear Chains of States Alexander Barkalov,Larysa Titarenko,Jacek Bieganowski,2017-06-24 This book discusses Moore finite state machines FSMs implemented with field programmable gate arrays FPGAs including look up table LUT elements and embedded memory blocks EMBs To minimize the number of LUTs in FSM logic circuits the authors propose replacing a state register with a state counter They also put forward an approach allowing linear chains of states to be created which simplifies the system of input memory functions and therefore decreases the number of LUTs in the resulting FSM circuit The authors combine this approach with using EMBs to implement the system of output functions microoperations This allows a significant decrease in the number of LUTs as well as eliminating a lot of interconnections in the FSM logic circuit As a rule it also reduces the area occupied by the circuit and diminishes the resulting power dissipation This book is an interesting and valuable resource for students and postgraduates in the area of computer science as well as for designers of digital systems that included complex control units **Finite State Machine Logic Synthesis for Complex Programmable Logic Devices** Robert Czerwinski,Dariusz Kania,2013-01-12 This book is a monograph devoted to logic synthesis and optimization for CPLDs CPLDs macrocell can also be interpreted as programmable AND fixed OR structure well known as PAL based structure The question is what should be done when the number of implicants representing function exceeds the number of product terms available in a logic block The answer is in the book Logic synthesis and optimization methods dedicated for PAL based structures are proposed The methods strive to find the optimum fit for the combinational logic and finite state machines to the structure of the logic device and aim at area and speed optimization The theoretical background and complete strategies are richly illustrated with examples and figures **Logic Synthesis for FPGA-Based Finite State Machines** Alexander Barkalov,Larysa Titarenko,Malgorzata Kolopienczyk,Kamil

Mielcarek,Grzegorz Bazydlo,2015-10-15 This book discusses control units represented by the model of a finite state machine FSM It contains various original methods and takes into account the peculiarities of field programmable gate arrays FPGA chips and a FSM model It shows that one of the peculiarities of FPGA chips is the existence of embedded memory blocks EMB The book is devoted to the solution of problems of logic synthesis and reduction of hardware amount in control units The book will be interesting and useful for researchers and PhD students in the area of Electrical Engineering and Computer Science as well as for designers of modern digital systems *Logic Synthesis for FPGA-Based Mealy Finite State Machines* Alexander Barkalov,Larysa Titarenko,Kazimierz Krzywicki,2024-12-04 This book is devoted to the logic synthesis of field programmable gate array FPGA based circuits of Mealy finite state machines FSM Three new methods of state assignment are proposed which allows obtaining FSM circuits required minimum amount of internal chip resources Logic Synthesis for FPGA Based Mealy Finite State Machines Structural Decomposition in Logic Design contains several original synthesis and optimization methods based on the structural decomposition of FPGA based FSM circuits developed by the authors To optimize FSM circuits the authors introduce the use of three methods of state assignment twofold extended and composite These methods allow for the creation of two or three level architectures of FSM circuits The authors also demonstrate how the proposed methods FSM architectures and synthesis methods can replace known solutions based on either functional decomposition or classical methods of structural decomposition The authors also show how these architectures have regular systems of interconnections and demonstrate positive features compared to methods based on functional decomposition including producing circuits with fewer elements that are faster and consume less power than their counterparts The book includes experimental results proving the efficiency of the proposed solutions and compares the numbers in Look up Tables LUTs showing the performance maximum operating frequency and power consumption for various methods of state assignment The audience for this book is students researchers and engineers specializing in computer science engineering electronics and telecommunications It will be especially useful for engineers working within the scope of algorithms hardware based software accelerators and control units and systems based on the use of FPGAs **Logic Synthesis for VLSI-Based Combined Finite State Machines** Alexander Barkalov,Larysa Titarenko,Kamil Mielcarek,Małgorzata Mazurkiewicz,Elżbieta Kawecka,2022-11-24 The book is devoted to design and optimization of control units represented by combined finite state machines CFSMs The CFSMs combine features of both Mealy and Moore FSMs Having states of Moore FSM they produce output signals of both Mealy and Moore types To optimize the circuits of CFSMs we propose to use optimization methods targeting both Mealy and Moore FSMs The book contains some original synthesis and optimization methods targeting hardware reduction in VLSI based CFSM circuits These methods take into account the peculiarities of both a CFSM model and a VLSI chip in use The optimization is achieved due to combining classical optimization methods with new methods proposed in this book These new methods are a mixed encoding of collections of microoperations and a

twofold state assignment in CFSMs All proposed methods target reducing the numbers of arguments in systems of Boolean functions representing CFSM circuits Also we propose to use classes of pseudoequivalent states of Moore FSMs to reduce the number of product terms in these systems The book includes a lot of examples which contributes to a better understanding of the features of the synthesis methods under consideration This is the first book entirely devoted to the problems associated with synthesis and optimization of VLSI based CFSMs We hope that the book will be interesting and useful for students and PhD students in the area of Computer Science as well as for designers of various digital systems We think that proposed CFSM models enlarge the class of models applied for implementation of control units with modern VLSI chips **Logic Synthesis for FSM-Based Control Units** Alexander Barkalov,Larysa Titarenko,2009-11-25 This book presents the hardware implementation of control algorithms represented by graph schemes of algorithm It includes new methods of logic synthesis and optimization for logic circuits of Mealy and Moore FSMs oriented on both ASIC and FPLD

Design and Implementation of Compiler Ravendra Singh,Vivek Sharma,Manish Varsheny,2009 About the Book This well organized text provides the design techniques of complier in a simple and straightforward manner It describes the complete development of various phases of complier with their imitation of C language in order to have an understanding of their application Primarily designed as a text for undergraduate students of Computer Science and Information Technology and postgraduate students of MCA Key Features Chapter1 covers all formal languages with their properties More illustration on parsing to offer enhanced perspective of parser and also more examples in e **Intelligent Information Processing and Web Mining** Mieczyslaw A. Klopotek,Slawomir T. Wierzchon,Krzysztof Trojanowski,2013-06-05 This volume contains articles accepted for presentation during The Intel ligent Information Processing and Web Mining Conference IIS IIPWM 04 which was held in Zakopane Poland on May 17 20 2004 This conference is a continuation of a series of 13 successful symposia and conferrences on Intel ligent Information Systems organized by the Institute of Computer Science of Polish Academy of Sciences devoted to new trends in broadly understood Artificial Intelligence The idea of organizing such meetings dates back to 1992 Our main in tention guided the first rather small audience workshop in the series was to resume the results gained in Polish scientific centers as well as contrast them with the research performed by Polish scientists working at the universities in Europe and USA and their foreign collaborators This idea proved to be attractive enough that we decided to continue such meetings As the years went by the workshops has transformed into regular symposia devoted to such fields like Machine Learning Knowledge Discovery Natural Language Processing Knowledge Based Systems and Reasoning and Soft Computing i e Fuzzy and Rough Sets Bayesian Networks Neural Networks and Evo lutionary Algorithms At present about 50 papers prepared by researches from Poland and other countries are usually presented This year conference devotes much more attention to the newest devel opments in the area of Artificial Intelligence related to broadly understood Web mining **RTL Hardware Design Using VHDL** Pong P. Chu,2006-04-20 The skills and guidance needed to master RTL hardware design

This book teaches readers how to systematically design efficient portable and scalable Register Transfer Level RTL digital circuits using the VHDL hardware description language and synthesis software Focusing on the module level design which is composed of functional units routing circuit and storage the book illustrates the relationship between the VHDL constructs and the underlying hardware components and shows how to develop codes that faithfully reflect the module level design and can be synthesized into efficient gate level implementation Several unique features distinguish the book Coding style that shows a clear relationship between VHDL constructs and hardware components Conceptual diagrams that illustrate the realization of VHDL codes Emphasis on the code reuse Practical examples that demonstrate and reinforce design concepts procedures and techniques Two chapters on realizing sequential algorithms in hardware Two chapters on scalable and parameterized designs and coding One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis it also examines the synthesis task from the perspective of the overall development process Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation verification and testing needs and can be easily incorporated into a larger system or reused Discussion is independent of technology and can be applied to both ASIC and FPGA devices With a balanced presentation of fundamentals and practical examples this is an excellent textbook for upper level undergraduate or graduate courses in advanced digital logic Engineers who need to make effective use of today s synthesis software and FPGA devices should also refer to this book

Modeling Time in Computing Carlo A. Furia,Dino Mandrioli,Angelo Morzenti,Matteo Rossi,2012-10-19 Models that include a notion of time are ubiquitous in disciplines such as the natural sciences engineering philosophy and linguistics but in computing the abstractions provided by the traditional models are problematic and the discipline has spawned many novel models This book is a systematic thorough presentation of the results of several decades of research on developing analyzing and applying time models to computing and engineering After an opening motivation introducing the topics structure and goals the authors introduce the notions of formalism and model in general terms along with some of their fundamental classification criteria In doing so they present the fundamentals of propositional and predicate logic and essential issues that arise when modeling time across all types of system Part I is a summary of the models that are traditional in engineering and the natural sciences including fundamental computer science dynamical systems and control theory hardware design and software algorithmic and complexity analysis Part II covers advanced and specialized formalisms dealing with time modeling in heterogeneous software intensive systems formalisms that share finite state machines as common ancestors Petri nets in many variants notations based on mathematical logic such as temporal logic process algebras and dual language approaches combining two notations with different characteristics to model and verify complex systems e g model checking frameworks Finally the book concludes with summarizing remarks and hints towards future developments and open challenges The presentation uses a rigorous yet not overly technical style appropriate for readers with heterogeneous backgrounds and each

chapter is supplemented with detailed bibliographic remarks and carefully chosen exercises of varying difficulty and scope The book is aimed at graduate students and researchers in computer science while researchers and practitioners in other scientific and engineering disciplines interested in time modeling with a computational flavor will also find the book of value and the comparative and conceptual approach makes this a valuable introduction for non experts The authors assume a basic knowledge of calculus probability theory algorithms and programming while a more advanced knowledge of automata formal languages and mathematical logic is useful   <u>Business Process Management</u> Marcello La Rosa,Peter Loos,Oscar Pastor,2016-09-18 This book constitutes the proceedings of the 14th International Conference on Business Process Management BPM 2016 held in Rio de Janeiro Brazil in September 2016 The focus of the conference covers a range of papers focusing on automated discovery conformance checking modeling foundations understandability of process representations runtime management and predictive monitoring The topics selected by the authors demonstrate an increasing interest of the research community in the area of process mining resonated by an equally fast growing uptake by different industry sectors   **Handbook of Schizophrenia Spectrum Disorders, Volume II** Michael S. Ritsner,2011-04-06 A few disorders have some of the same symptoms as schizophrenia including schizoaffective disorders schizophreniform disorder schizotypal and schizoid personality disorders delusional disorder and autism schizophrenia spectrum disorders Since the 2000 there has been significant progress in our understanding of the early presentations assessment suspected neuropathology and treatment of these disorders Recent technological breakthroughs in basic sciences hold promise for advancing our understanding of the pathophysiology of schizophrenia spectrum disorders This collective monograph reviewers recent researches regarding the origins onset course and outcome of schizophrenia spectrum disorders In particular this book will be illustrate new developments in terms of conceptual models and research methodology genetics and genomics brain imaging and neurochemical studies neurophysiology and information processing in schizophrenia spectrum disorders patients Also will be highlighted new developments in our understanding of the childhood psychosis prodromal and first episode states in treatment and rehabilitation Thus the purpose of this book is to provide up to date overview of the rapid advances made in the clinical and basic science studies supporting our understanding of the relationship between cerebral processes and clinical cognitive and other presentations of the schizophrenia spectrum disorders In addition this book aims to monitor important research developments which may be relevant to treatment and rehabilitation of patients   **Applications of Zero-Suppressed Decision Diagrams** Jon T. Butler,Tsutomu Sasao,2022-05-31 A zero suppressed decision diagram ZDD is a data structure to represent objects that typically contain many zeros Applications include combinatorial problems such as graphs circuits faults and data mining This book consists of four chapters on the applications of ZDDs The first chapter by Alan Mishchenko introduces the ZDD It compares ZDDs to BDDs showing why a more compact representation is usually achieved in a ZDD The focus is on sets of subsets and on sum of

products SOP expressions Methods to generate all the prime implicants PIs and to generate irredundant SOPs are shown A list of papers on the applications of ZDDs is also presented In the appendix ZDD procedures in the CUDD package are described The second chapter by Tsutomu Sasao shows methods to generate PIs and irredundant SOPs using a divide and conquer method This chapter helps the reader to understand the methods presented in the first chapter The third chapter by Shin Ichi Minato introduces the frontier based method that efficiently enumerates certain subsets of a graph The final chapter by Shinobu Nagayama shows a method to match strings of characters This is important in routers for example where one must match the address information of an internet packet to the proprer output port It shows that ZDDs are more compact than BDDs in solving this important problem Each chapter contains exercises and the appendix contains their solutions Table of Contents Preface Acknowledgments Introduction to Zero Suppressed Decision Diagrams Efficient Generation of Prime Implicants and Irredundant Sum of Products Expressions The Power of Enumeration BDD ZDD Based Algorithms for Tackling Combinatorial Explosion Regular Expression Matching Using Zero Suppressed Decision Diagrams Authors and Editors Biographies Index **Logic Synthesis for FPGA-Based Control Units** Alexander Barkalov,Larysa Titarenko,Kamil Mielcarek,Sławomir Chmielewski,2020-01-08 This book focuses on control units which are a vital part of modern digital systems and responsible for the efficiency of controlled systems The model of a finite state machine FSM is often used to represent the behavior of a control unit As a rule control units have irregular structures that make it impossible to design their logic circuits using the standard library cells Design methods depend strongly on such factors as the FSM used specific features of the logic elements implemented in the FSM logic circuit and the characteristics of the control algorithm to be interpreted This book discusses Moore and Mealy FSMs implemented with FPGA chips including look up table elements LUT and embedded memory blocks EMB It is crucial to minimize the number of LUTs and EMBs in an FSM logic circuit as well as to make the interconnections between the logic elements more regular and various methods of structural decompositions can be used to solve this problem These methods are reduced to the presentation of an FSM circuit as a composition of different logic blocks the majority of which implement systems of intermediate logic functions different and much simpler than input memory functions and FSM output functions The structural decomposition results in multilevel FSM circuits having fewer logic elements than equivalent single level circuits The book describes well known methods of structural decomposition and proposes new ones examining their impact on the final amount of hardware in an FSM circuit It is of interest to students and postgraduates in the area of Computer Science as well as experts involved in designing digital systems with complex control units The proposed models and design methods open new possibilities for creating logic circuits of control units with an optimal amount of hardware and regular interconnections *Compiler Construction* , **Languages for Digital Embedded Systems** Stephen A. Edwards,2012-12-06 Appropriate for use as a graduate text or a professional reference Languages for Digital Embedded Systems is the first detailed broad survey of

hardware and software description languages for embedded system design Instead of promoting the one language that will solve all design problems which does not and will not ever exist this book takes the view that different problems demand different languages and a designer who knows the spectrum of available languages has the advantage over one who is trapped using the wrong language Languages for Digital Embedded Systems concentrates on successful widely used design languages with a secondary emphasis on those with significant theoretical value The syntax semantics and implementation of each language is discussed since although hardware synthesis and software compilation technology have steadily improved coding style still matters and a thorough understanding of how a language is synthesized or compiled is generally necessary to take full advantage of a language Practicing designers graduate students and advanced undergraduates will all benefit from this book It assumes familiarity with some hardware or software languages but takes a practical descriptive view that avoids formalism

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