SYSTEMATEC MODULLING AND ANGLYSIS OF TELESCOM FRONTENDS AND THERE BUILDING BUCKES

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Libin Yao, Michiel Steyaert, Willy M. C. Sansen

Systematic Modeling and Analysis of Telecom Frontends and their Building Blocks Piet Vanassche, Georges Gielen, Willy M. C. Sansen, 2005-09-01 To meet the demands of today s highly competitive market analog electronics designers must develop their IC designs in a minimum of time The difference between first and second time right seriously affects a company s share of the market Analog designers are therefore in need for structured design methods together with the theory and tools to support them especially when pushing the performance limits in high performance designs Systematic Modeling and Analysis of Telecom Frontends and Their Building Blocks aims to help designers in speeding up telecommunication frontend design by offering an in depth understanding of the frontend's behavior together with methods and algorithms that support designers in bringing this understanding to practice The book treats topics such as time varying phase locked loop stability noise in mixing circuits oscillator injection locking oscillator phase noise behavior harmonic oscillator dynamics and many more In doing so it always starts from a theoretical foundation that is both rigorous and general Phase locked loop and mixer analysis for example are grounded upon a general framework for time varying small signal analysis Likewise analysis of harmonic oscillator transient behavior and oscillator phase noise analysis are treated as particular applications of a general framework for oscillator perturbation analysis In order to make the book as easy to read as possible all theory is always accompanied by numerous examples and easy to catch intuitive explanations As such the book is suited for both computer aided design engineers looking for general theories and methods either as background material or for practical implementation in tools as well as for practicing circuit designers looking for help and insight in dealing with a particular application or a particular high performance design problem Design of Very High-Frequency Multirate Switched-Capacitor Circuits Seng-Pan U, Rui Paulo Martins, José Epifânio da Franca, 2006 Design of Very High Frequency Multirate Switched Capacitor Circuits presents the theory and the corresponding CMOS implementation of the novel multirate sampled data analog interpolation technique which has its great potential on very high frequency analog frond end filtering due to its inherent dual advantage of reducing the speed of data converters and DSP core together with the specification relaxation of the post continuous time filtering This technique completely eliminates the traditional phenomenon of sampled and hold frequency shaping at the lower input sampling rate Also in order to tackle physical IC imperfections at very high frequency the state of the art circuit design and layout techniques for high speed Switched Capacitor SC circuits are comprehensively discussed Optimum circuit architecture tradeoff analysis Simple speed and power trade off analysis of active elements High order filtering response accuracy with respect to capacitor ratio mismatches Time interleaved effect with respect to gain and offset mismatch Time interleaved effect with respect to timing skew and random jitter with non uniformly holding Stage noise analysis and allocation scheme Substrate and supply noise reduction Gain and offset compensation techniques High bandwidth low power amplifier design and layout Very low timing skew multiphase

generation Two tailor made optimum design examples in CMOS are presented The first one achieves a 3 stage 8 fold SC interpolating filter with 5 5MHz bandwidth and 108MHz output sampling rate for a NTSC PAL CCIR 601 digital video at 3 V Another is a 15 tap 57MHz SC FIR bandpass interpolating filter with 4 fold sampling rate increase to 320MHz and the first time embedded frequency band up translation for DDFS system at 2 5V The corresponding chip prototype achieves so far the highest operating frequency highest filter order and highest center frequency with highest dynamic range under the lowest supply voltage when compared to the previously reported high frequency SC filters in CMOS CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom Rocío Río Fernández, Fernando Medeiro Hidalgo, Belén Pérez Verdú, José Manuel Rosa Utrera, Ángel Rodríguez-Vázguez, 2006-09-03 Institutional book not really for bookstore catalogue The book contains valuable information structured to provide insight on how to design SC sigma delta modulators It presents architectures circuits models methods and practical considerations for the design of high performance low pass switched capacitor SC sigma delta A D interfaces for mixed signal CMOS ASICs The main focus of the book is on cascade architectures It differs from other books in the complete in depth coverage of SC circuit errors **High-Speed Photodiodes in Standard CMOS** Technology Sasa Radovanovic, Anne-Johan Annema, Bram Nauta, 2006-10-11 High speed Photodiodes in Standard CMOS Technology describes high speed photodiodes in standard CMOS technology which allow monolithic integration of optical receivers for short haul communication For short haul communication the cost aspect is important and therefore it is desirable that the optical receiver can be integrated in the same CMOS technology as the rest of the system If this is possible then ultimately a singe chip system including optical inputs becomes feasible eliminating EMC and crosstalk problems while data rate can be extremely high The problem of photodiodes in standard CMOS technology it that they have very limited bandwidth allowing data rates up to only 50Mbit per second High speed Photodiodes in Standard CMOS Technology first analyzes the photodiode behaviour and compares existing solutions to enhance the speed After this the book introduces a new and robust electronic equalizer technique that makes data rates of 3Gb s possible without changing the manufacturing technology The application of this technique can be found in short haul fibre communication optical printed circuit boards but also photodiodes for laser disks Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS Libin Yao, Michiel Steyaert, Willy M. C. Sansen, 2006-02-06 this book is not suitable for the bookstore catalogue Design of Wireless Autonomous Datalogger IC's Wim Claes, Willy M Sansen, Robert Puers, 2006-03-30 Design of Wireless Autonomous Dataloggers IC s reveals the state of the art in the design of complex dataloggers with a special focus on low power consumption The emphasis is on autonomous dataloggers for stand alone applications with remote reprogrammability The book starts with a comprehensive introduction on the most important design aspects and trade offs for miniaturized low power telemetric dataloggers After the general introduction follows an in depth case study of an autonomous CMOS datalogger IC for the registration of in vivo loads on oral implants After tackling the design of the datalogger on the system

level the design of the different building blocks is elaborated in detail with emphasis on low power A clear overview of the operation the implementation and the most important design considerations of the building blocks to achieve optimal system performance is given Design of Wireless Autonomous Dataloggers IC s discusses the design of correlated double sampling amplifiers and sample and holds binary weighted current steering DACs successive approximation ADCs and relaxation clock oscillators and can also be used as a manual for the design of these building blocks Design of Wireless Autonomous Dataloggers IC s covers the complete design flow of low power miniaturized autonomous dataloggers with a bi directional wireless link and on board data processing while providing detailed insight into the most critical design issues of the different building blocks It will allow you to design complex dataloggers faster It is essential reading for analog design engineers and researchers in the field of miniaturized dataloggers and is also suitable as a text for an advanced course on the Matching Properties of Deep Sub-Micron MOS Transistors Jeroen A. Croon, Willy M Sansen, Herman E. Maes, 2006-06-20 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET For analog circuits this determines the trade off between speed power accuracy and yield Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits The matching properties of MOSFETs are studied at several levels of abstraction A simple and physics based model is presented that accurately describes the mismatch in the drain current The model is illustrated by dimensioning the unit current cell of a current steering D A converter The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated This leads to a refinement of the generally applied 1 area law In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance The impact of process parameters on the matching properties is discussed The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor Matching Properties of Deep Sub Micron MOS Transistors is aimed at device physicists characterization engineers technology designers circuit designers or anybody else interested in **Dynamic Characterisation of Analogue-to-Digital Converters** Dominique the stochastic properties of the MOSFET Dallet, José Machado da Silva, 2006-03-08 The Analogue to digital converter ADC is the most pervasive block in electronic systems With the advent of powerful digital signal processing and digital communication techniques ADCs are fast becoming critical components for system's performance and flexibility Knowing accurately all the parameters that characterise their dynamic behaviour is crucial on one hand to select the most adequate ADC architecture and characteristics for each end application and on the other hand to understand how they affect performance bottlenecks in the signal processing chain

Dynamic Characterisation of Analogue to Digital Converters presents a state of the art overview of the methods and procedures employed for characterising ADCs dynamic performance behaviour using sinusoidal stimuli The three classical methods histogram sine wave fitting and spectral analysis are thoroughly described and new approaches are proposed to circumvent some of their limitations This is a must have compendium which can be used by both academics and test professionals to understand the fundamental mathematics underlining the algorithms of ADC testing and as an handbook to help the engineer in the most important and critical details for their implementation **Wideband Low Noise Amplifiers** Exploiting Thermal Noise Cancellation Federico Bruccoleri, Eric Klumperink, Bram Nauta, 2006-03-30 Low Noise Amplifiers LNAs are commonly used to amplify signals that are too weak for direct processing for example in radio or cable receivers Traditionally low noise amplifiers are implemented via tuned amplifiers exploiting inductors and capacitors in resonating LC circuits This can render very low noise but only in a relatively narrow frequency band close to resonance There is a clear trend to use more bandwidth for communication both via cables e g cable TV internet and wireless links e g satellite links and Ultra Wideband Band Hence wideband low noise amplifier techniques are very much needed Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation explores techniques to realize wideband amplifiers capable of impedance matching and still achieving a low noise figure well below 3dB This can be achieved with a new noise cancelling technique as described in this book By using this technique the thermal noise of the input transistor of the LNA can be cancelled while the wanted signal is amplified The book gives a detailed analysis of this technique and presents several new amplifier circuits This book is directly relevant for IC designers and researchers working on integrated transceivers Although the focus is on CMOS circuits the techniques can just as well be applied to other IC technologies e g bipolar and GaAs and even in discrete component technologies Sigma Delta A/D Conversion for Signal Conditioning Kathleen Philips, Arthur H.M. van Roermund, 2006-05-05 1 1 Background Moore's Law predicts a decrease by a factor of two in the feature size of CMOS te nology every three years and has been valid for years It implies a doubling of the eration speed and a four times higher transistor count per unit of area every three years The combination leads to an eight times higher processing capability per unit of area This on going miniaturization allows the integration of complex electronic systems with millions of transistors Very Large Scale Integration and enables the integration of el tronic systems An electronic system A generic picture of an integrated electronic system is shown in g 1 1 The heart of the system is the signal processing core This core supports a wide variety of functions such as customization and programmability of multiple applications channel coding the de nition of the user interface etc These functions are enabled by DSP a controller CPU and various blocks of memory In advanced ICs these blocks provide almost all signal processing and usually dominate in the overall power and area consumption of integrated systems The huge data rates involved require high speed busses for communication between these blocks A power management unit fuels the system by providing the propriate supply voltages and currents Calibration

Techniques in Nyquist A/D Converters Hendrik van der Ploeg, Bram Nauta, 2006-09-13 This book analyses different A D converter architectures with an emphasis on the maximum achievable power efficiency. It also provides an accessible overview of the state of the art in calibration techniques for Nyquist A D converters The calibration techniques presented are applicable to other analog to digital systems such as those applied in integrated receivers They allow implementation without introducing a speed or power penalty Wide-Bandwidth High Dynamic Range D/A Converters Konstantinos Doris, Arthur H.M. van Roermund, Domine Leenaerts, 2006-01-12 IGH SPEED Digital to Analog D A converters are essential components in digi Htal communication systems providing the necessary conversion of signals encoding information in bits to signals encoding information in their amplitude vs time domain characteristics. In general they are parts of a larger system the interface which c sists of several signal conditioning circuits Dependent on where the converter is located within the chain of circuits in the interface signal processing operations are partitioned in those realized with digital techniques and those with analog The rapid evolution of CMOS technology has established implicit and explicite trends related to the interface and in particular to the D A converter The implicit relationship comes via the growth of digital systems First it is a global trend with respect to all interface circuits that increasing operating frequencies of digital systems place a similar demand for the interface circuits The second trend takes place locally within the int face Initially the D A converter was placed at the beginning of the interface chain and all signal conditioning was implemented in the analog domain after the D A conversion The increasing exibility and robustness of digital signal processing shifted the D A converter closer to the end point of the chain where the demands for high quality high frequency operation are very high Adaptive Low-Power Circuits for Wireless Communications Aleksandar Tasic, Wouter A. Serdijn, John R. Long, 2007-03-06 Adaptive radio transceivers require a comprehensive theoretical framework in order to optimize their performance Adaptive Low Power Circuits for Wireless Communications provides this framework with a discussion of joint optimization of Noise Figure and Input Intercept Point in receiver systems Original techniques to optimize voltage controlled oscillators and low noise amplifiers to minimize their power consumption while maintaining adequate system performance are also provided. The experimental results presented at the end of the book confirm the utility of the proposed techniques RF Power Amplifiers for Mobile Communications Patrick Reynaert, Michiel Steyaert, 2006-11-18 This book tackles both high efficiency and high linearity power amplifier PA design in low voltage CMOS With its emphasis on theory design and implementation the book offers a guide for those actively involved in the design of fully integrated CMOS wireless transceivers Offering mathematical background as well as intuitive insight the book is essential reading for RF design engineers and researchers and is also suitable as a text book

Advanced Design Techniques for RF Power Amplifiers Anna N. Rudiakova, Vladimir Krizhanovski, 2006-09-09 Advanced Design Techniques for RF Power Amplifiers main aim is to provide the reader with a deep analysis of theoretical aspects modelling and design strategies of RF high efficiency power amplifiers Advanced Design Techniques for RF Power Amplifiers

begins with an analytical review of current state of the problem Then it moves to the theoretical analysis of BIT class F power amplifier near transition frequency and presents the necessary realization conditions. The next part concerns the practical verification and demonstration of the theoretical results It is followed by the part devoted to the output networks of high efficiency power ampifiers The novel type of photonic band gap structure providing improved characteristics both in the pass and stop bands is proposed Finally the fifth harmonic peaking class F power amplifier design based on the above structure is **Precision Temperature Sensors in CMOS Technology** Micheal A.P. Pertijs, Johan Huijsing, 2006-12-06 The low cost and direct digital output of CMOS smart temperature sensors are important advantages compared to conventional temperature sensors This book addresses the main problem that nevertheless prevents widespread plication of CMOS smart temperature sensors their relatively poor absolute accuracy Several new techniques are introduced to improve this accuracy The effectiveness of these techniques is demonstrated using three prototypes The nal prototype achieves an inaccuracy of 0 1 C over the military t perature range which is a signi cant improvement in the state of the art Since smart temperature sensors have been the subject of academic and industrial research for more than two decades an overview of existing knowledge and techniques is also provided throughout the book Inthisintroductorychapter themotivation and objectives of this work are scribed. This is followed by a review of the basic operating principles of CMOS smart temperature sensors and a brief overview of previous work. The ch lenges are then described that need to be met in order to improve the accuracy of CMOS smart temperature sensors while maintaining their cost advantage Finally the structure of the rest of the book is introduced CMOS Current-Mode Circuits for Data Communications Fei Yuan, 2007-04-26 Current mode circuits where information is represented by the branch currents of the circuits rather than the nodal voltages as of voltage mode circuits possess many unique and attractive characteristics over their voltage mode counterparts including a small nodal time constant high current swing in the presence of a low supply voltage reduced distor tion a low input impedance a high output impedance less sensitive to switching noise and better ESD immunity CMOS current mode circuits have found increasing applications in telecommunication sys tems instrumentation analog signal processing multiprocessors high speed computer interfaces and the backplane of complex electronic sys tems This book deals with the analysis and design of continuous time CMOS current mode circuits for data communications over wire chan nels CMOS current mode sampled data networks such as switch current circuits and current mode logic circuits are excluded The book is organized as the followings Chapter 1 examines the distinct characteristics of ideal voltage mode and current mode circuits The topology duaUty of these two classes of circuits is investigated using the concept of inter reciprocity and adjoint network A critical comparison of the input and output impedances bandwidth slew rate propagation delay signal swing supply voltage sensitivity and ESD sensitivity of voltage mode and current mode cir cuits is provided Chapter 2 investigates design techniques that improve the perfor mance of low voltage current mode circuits including input impedance reduction output

impedance boosting bandwidth enhancement mis match compensation power consumption reduction and swing improve ment Chapter 3 investigates the modeling of wire channels **IQ Calibration Techniques for CMOS Radio Transceivers** Sao-Jie Chen, Yong-Hsiang Hsieh, 2006-09-22 The 802 11n wireless standard uses 64 state guadrature amplitude modulation 64 QAM to achieve higher spectral efficiency Consequently the transmitter and receiver require a higher signal to noise ratio with the same level of error rate performance This book offers a fully analog compensation technique without baseband circuitry to control the calibration process Using an 802 11g transceiver design as an example it describes in detail an auto calibration mechanism for I Q gains and phases imbalance Analog Circuit Design Techniques at 0.5V Shouri Chatterjee, 2007-08-02 This book tackles challenges for the design of analog integrated circuits that operate from ultra low power supply voltages down to 0 5V Coverage demonstrates the signal processing circuit and circuit biasing approaches through the design of operational transconductance amplifiers OTAs These amplifiers are then used to build analog system functions including continuous time filter and a sample and hold amplifier High-Level Modeling and Synthesis of Analog Integrated Systems Ewout S. J. Martens, Georges Gielen, 2008-01-03 As the miniaturization of semiconductor technology continues electronic s tems on chips o er a more extensive and more complex functionality with better performance higher frequencies and less power consumption Whereas digital designers can take full advantage of the availability of design auto tiontoolstobuildhugesystems thelackofsupportbycomputerprogramsfor di erent abstraction levels makes analog design a time consuming handcraft which limits the possibilities to implement large systems Various approaches for ndingoptimal values for the parameters of analog cells like opamps have been investigated since the mid 1980s and they have made their entrance in commercial applications However a larger impact on the performance is pected if tools are developed which operate on a higher abstraction level and consider multiple architectural choices to realize a particular functionality In this book the opportunities conditions problems solutions and systematic methodologies for this new generation of analog CAD tools are examined Theoutlineofthisbookisasfollows Inthe rstpart thecharacteristics of the analog design process are systematically analyzed and several approaches for automated analog synthesis are summarized Comparison of their prop ties with the requirements for high level synthesis of analog and mixed signal systems results in a new design paradigm the high level design ow based on generic behavior This design approach involves a modeling strategy using generic behavioral models and a synthesis strategy leading to the exploration of a heterogeneous design space containing di erent architectures The modeling strategy is further elaborated in Part II

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