

2) Using loops already chosen as inhibitions, attempt to cover remaining ones, and/or zeros.

3) Repeat (2) until all ones and zeros are covered. Last level of loops (for NAND) must be zeros (must be an OR) so if last level is ones, inhibit the ones from unity, i.e., complement the output.

These rules are simple but are no measure of the complexity and suitability they may beget in application since they give little in the way of guidance.

Example 6.4. In Figure 6.25 a step by step example is worked. In Figure 6.25a, the loop B, C inhibited by A, C is chosen, and loop A inhibited by A, C is chosen. This gets us all but one of the ones. We can get the remaining term $\bar{A}BC$ by getting the remaining zeros looped and inhibiting unity, the whole map with all the zero loops. Two zeros are covered by the loop of Figure 6.25b where loop B is inhibited by the one loops generated in Figure 6.25a. The final zero is achieved in Figure 6.25c. Inhibiting the whole map with the zero loops yields all the ones (Figure 6.25d) but to end on a loop of zeros we inhibit the one's from unity, i.e., we complement the result.

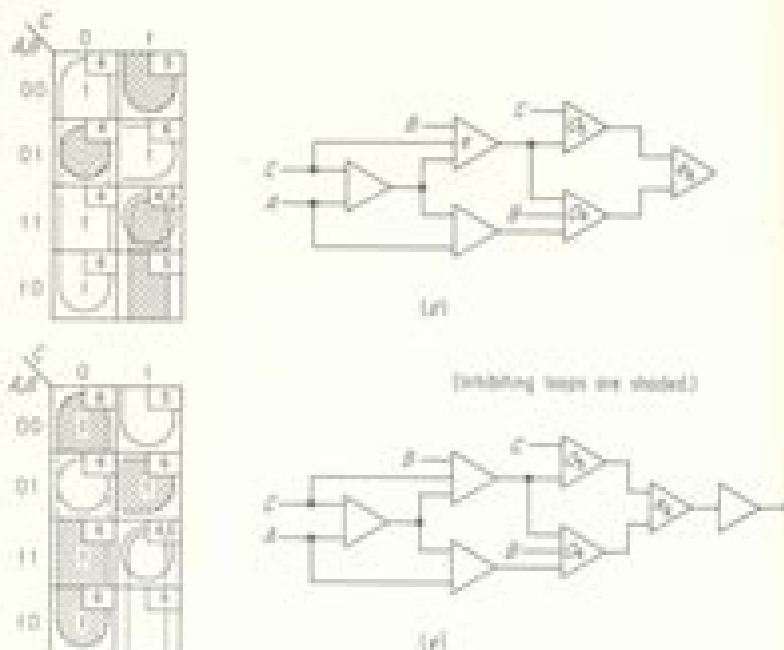


Figure 6.25 (a, b, c, d).

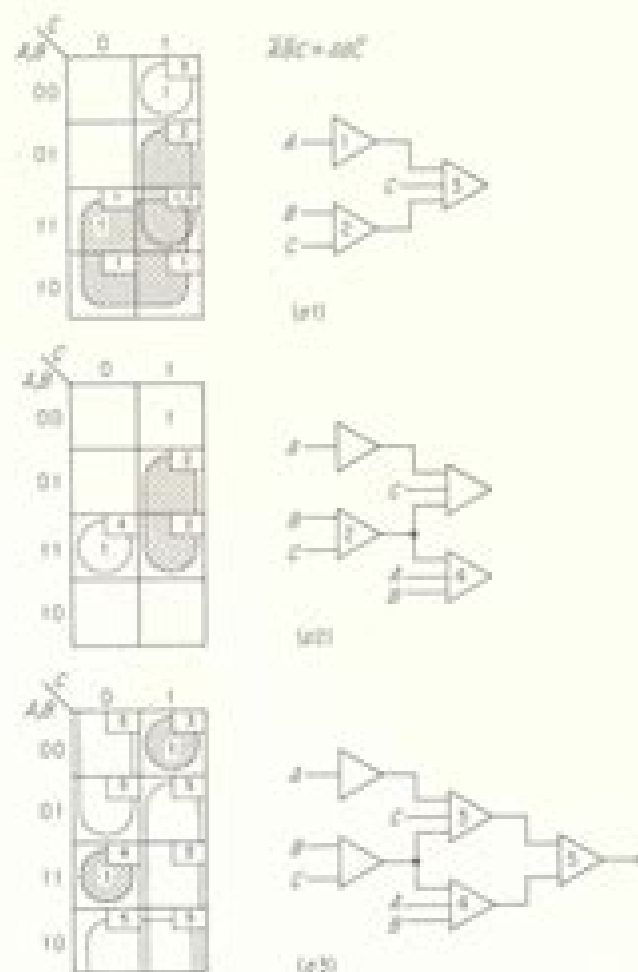


Figure 6.26 (a1, a2, a3). Two map factorizations of a single three-variable function.

The Logic Design Of Transistor Digital Computers

IM Harris



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