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Smart Power Ics Technologies And Applications

**Johan Huijsing, Michiel Steyaert, Arthur
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necessity for lateral power transistors by a top down approach First it presents typical energy conversion applications in modern industrial automotive and consumer electronics Next it introduces common circuit topologies suitable for these applications and discusses the feasibility for monolithic integration Finally the combination of power and logic functionality on a single chip is motivated and the requirements and limitations for the power semiconductor devices are deduced The second part describes the evolution of lateral power transistors over the past decades from the simple pin type concept to double acting RESURF topologies It describes the principle of operation for these LDMOS devices and discusses limitations of lateral power devices Moreover figures of merit are presented which can be used to evaluate the performance of the novel lateral power transistors described in this book with respect to the LDMOS devices In the last part the fundamental physical concepts including charge compensation and trench gate topologies are discussed Also the status of research in LDMOS devices on silicon carbide is presented Advantages and drawbacks for each of these integration approaches are summarized and the feasibility with respect to power electronic applications is evaluated

Analog Circuit Design Johan Huijsing, Michiel Steyaert, Arthur H.M. van Roermund, 2013-03-20 Analog Circuit Design contains the contribution of 18 experts from the 13th International Workshop on Advances in Analog Circuit Design It is number 13 in the successful series of Analog Circuit Design It provides 18 excellent overviews of analog circuit design in Sensor and Actuator Interfaces Integrated High Voltage Electronics and Power Management and Low Power and High Resolution ADC s Analog Circuit Design is an essential reference source for analog circuits designers and researchers wishing to keep abreast with the latest developments in the field The tutorial coverage also makes it suitable for use in an advanced design course

ESD Protection Device and Circuit Design for Advanced CMOS Technologies Oleg Semenov, Hossein Sarbishaei, Manoj Sachdev, 2008-04-26 ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design VLSI reliability and testing domains As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry the demand for graduates with a basic knowledge of ESD is also increasing Today there is a significant demand to educate the circuits design and reliability teams on ESD issues This book makes an attempt to address the ESD design and implementation in a systematic manner A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance This methodology described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths

Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies Stephan Henzler, 2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and

threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side

Guide to State-of-the-Art Electron Devices
Joachim N. Burghartz, 2013-03-19 Winner 2013 PROSE Award Engineering and Technology Concise high quality and comparative overview of state of the art electron device development manufacturing technologies and applications Guide to State of the Art Electron Devices marks the 60th anniversary of the IRE electron devices committee and the 35th anniversary of the IEEE Electron Devices Society as such it defines the state of the art of electron devices as well as future directions across the entire field Spans full range of electron device types such as photovoltaic devices semiconductor manufacturing and VLSI technology and circuits covered by IEEE Electron and Devices Society Contributed by internationally respected members of the electron devices community A timely desk reference with fully integrated colour and a unique lay out with sidebars to highlight the key terms Discusses the historical developments and speculates on future trends to give a more rounded picture of the topics covered A valuable resource R engineers in the semiconductor industry applied scientists circuit designers Masters students in power electronics and members of the IEEE Electron Device Society

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