Real-Time Digital Signal Processing in a Mixed-Signal LSI Test System

In test subsystems based on digital signal processing, the HP 9493 test system emulates the analog and digital signals of the device under test, thereby reducing test time and increasing test coverage compared to a memory-based test system.

by Keita Gunji

Complex mixed-signal integrated circuits are used more and more frequently to realize many complex functions needed for applications such as telecommunications, serve centrel, and image processing. Testing of these ICs is much more difficult than for traditional ICs because of the integration of complex functions and synchronized interactions between blocks. Governtional IC testing methods cannot provide both high test throughput and high test quality for these devices. At-speed signal processing by synchronized distributed subsystems is required to perform functional testing of complex mixed-signal devices. Also required is a programming style that is straightforward and allows flexible control of signal and data flow in the test subsystems.

DSP-based LSI testers can be classified as having one of two types of architecture according to the location of the signal processing units (SPU): centralized or distributed. In the distributed type, SPUs are distributed among the individual subsystems. Usually, each SPU cannot manage a large amount of data and the processing speed of each SPU is slower than that of a centralized SPU. Programming is more difficult because the SPUs are not strongly coupled to the GPU, so the control layer between the CPU and the SPUs is more complicated. On the other hand, the distributed type makes it possible to process data in the subsystems and enables at-speed emulation of IC functions, which is required to test mixed-signal devices.

To meet the needs of complex mixed-signal testing, the HP 9495 mixed-signal LSI test system is based on distributed digital signal processors (DSPs). In each test subsystem is a Motorola DSP950002 chip, which runs at 52 MHz and performs 32-bit floating-point operations. The DSP modules are connected by data transmission paths for data sharing. A flexible programming language directs the DSPs to generate and analyze test signals.

The HP 9495 architecture allows digital and analog signal processing completion times on the order of microseconds to ensure the quality and throughput of dynamic signals and data operations for the device under test (DUT). Precise timing synchronization of all subsystems makes it possible to distribute operations among the DSP modules.

Compared to a memory-based test system, the HP 9493's distributed DSP architecture reduces test time and increases test coverage for complex mixed-signal devices. To generate

an analog waveform, the conventional memory-based system must compute and store discrete time data for the entire waveform before generating it. This takes time and may require so much memory that the functions of a complex device may not be tested completely because of the memory cost. In contrast, the DSP-based HIP 9403 prepares the discrete time data in real time using a much smaller amount of waveform memory.

Architecture

Fig. 1 shows the HP 9493 system architecture, which allows synchronous and asynchronous control of the analog and digital subsystems and the distributed DSP in each subsystem. This distributed architecture consists of a tester controller, which controls all test subsystems, a master clock subsystem, two test heads, and test subsystems. The test subsystems include digital subsystems, which generate and fetch digital patterns and signals, arbitrary waveform generator subsystems, and waveform digitaer subsystems.

In each test subsystem are a DSP module, a sequencer, and a memory block. Each DSP module has a data transmission path. The DSP modules operate on data or signals according to instructions loaded from the tester controller, and the start and stop operations are synchronized by the master sequencer or tester controller. The master sequencer precisely synchronizes the timing of the other sequencers.

The DSP96002 manages the memory block. Data can also be stored in high-speed memory in the DSP module to reduce memory access time, which increases the processing speed of the DSP90002. The sequencer in each subsystem controls address generation and the timing of data fetch or generation between the memory block and the signal input or output for memory-based testing.

The advantages of this architecture are real-time signal emulation and shared signal processing. Test throughput is more than double the capability of conventional LSI testers, and IGs can be evaluated by at-speed functional tests. Data can be transmitted between DSP modules without CPU intervention, which allows synchronous and concurrent operation and sharing of signals from the DRIT.

The DSP module in the digital subsystem can fetch and generate up to 52-bit digital test data. The test data is directly connected to the data bus of the DSP96002. Data can be

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Test and Design-for-Testability in Mixed-Signal Integrated Circuits Jose Luis Huertas Díaz, 2010-02-23 Test and Design for Testability in Mixed Signal Integrated Circuits deals with test and design for test of analog and mixed signal integrated circuits Especially in System on Chip SoC where different technologies are intertwined analog digital sensors RF test is becoming a true bottleneck of present and future IC projects Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time cost and proficiency Although it is recognized as a key issue for developing complex ICs there is still a lack of structured references presenting the major topics in this area. The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students Since this is an active research field a comprehensive state of the art overview is very valuable introducing the main problems as well as the ways of solution that seem promising emphasizing their basis strengths and weaknesses In essence several topics are presented in detail First of all techniques for the efficient use of DSP based test and CAD test tools Standardization is another topic considered in the book with focus on the IEEE 1149 4 Also addressed in depth is the connecting design and test by means of using high level behavioural description techniques specific examples are given Another issue is related to test techniques for well defined classes of integrated blocks like data converters and phase locked loops Besides these specification driven testing techniques fault driven approaches are described as they offer potential solutions which are more similar to digital test methods Finally in Design for Testability and Built In Self Test two other concepts that were taken from digital design are introduced in an analog context and illustrated for the case of integrated filters. In summary the purpose of this book is to provide a glimpse on recent research results in the area of testing mixed signal integrated circuits specifically in the topics mentioned above Much of the work reported herein has been performed within cooperative European Research Projects in which the authors of the different chapters have actively collaborated It is a representative snapshot of the current state of Oscillation-Based Test in Mixed-Signal Circuits Gloria Huertas Sánchez, Diego Vázguez the art in this emergent field García de la Vega, Adoración Rueda Rueda, Jose Luis Huertas Díaz, 2007-06-03 Oscillation Based Test in Mixed Signal Circuits presents the development and experimental validation of the structural test strategy called Oscillation Based Test OBT in short The results here presented allow to assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits **Computer-Aided Design of Analog Integrated Circuits and Systems Rob A.** Rutenbar, Georges G. E. Gielen, 2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are

moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck Efficient Testability Design Methodology for Analog/mixed Signal Integrated Circuits Cheng-Ping Wang,1997

An Introduction to Mixed-signal IC Test and Measurement Gordon W. Roberts, Friedrich Taenzler, Mark Burns, 2012 With the proliferation of complex semiconductor devices containing digital analog mixed signal and radio frequency circuits the economics of test has come to the forefront and today s engineer needs to be fluent in all four circuit types Having access to a book that covers these topics will help the evolving test engineer immensely and will be an invaluable resource In addition the second edition includes lengthy discussion on RF circuits high speed I Os and probabilistic reasoning Appropriate for the junior senior university level this textbook includes hundreds of examples exercises and problems **Essentials of** Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems on a chip which include digital memory and mixed signal subsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers *Low-power HF Microelectronics*

Gerson A. S. Machado, 1996 This book brings together innovative modelling simulation and design techniques in CMOS SOI GaAs and BJT to achieve successful high yield manufacture for low power high speed and reliable by design analogue and mixed mode integrated systems Emerging Trends in Technological Innovation Luis M. Camarinha-Matos, Pedro Pereira, Luis Ribeiro, 2010-02-26 Identifying Emerging Trends in Technological Innovation Doctoral programs in science and engineering are important sources of innovative ideas and techniques that might lead to new products and technological innovation Certainly most PhD students are not experienced researchers and are in the process of learning how to do research Nevertheless a number of empiric studies also show that a high number of technological innovation ideas are produced in the early careers of researchers The combination of the eagerness to try new approaches and directions of young doctoral students with the experience and broad knowledge of their supervisors is likely to result in an important pool of innovation potential The DoCEIS doctoral conference on Computing Electrical and Industrial En neering aims at creating a space for sharing and discussing ideas and results from doctoral research in these inter related areas of engineering Innovative ideas and hypotheses can be better enhanced when presented and discussed in an encouraging and open environment DoCEIS aims to provide such an environment releasing PhD students from the pressure of presenting their propositions in more formal contexts Mixed-Signal Circuits Thomas Noulis, 2018-09-03 Mixed Signal Circuits offers a thoroughly modern treatment of integrated circuit design in the context of mixed signal applications Featuring chapters authored by leading experts from industry and academia this book Discusses signal integrity and large scale simulation verification and testing Demonstrates advanced design techniques that enable digital circuits and sensitive analog circuits to coexist without any compromise Describes the process technology needed to address the performance challenges associated with developing complex mixed signal circuits Deals with modeling topics such as reliability variability and crosstalk that define pre silicon design methodology and trends and are the focus of companies involved in wireless applications Develops methods to move analog into the digital domain quickly minimizing and eliminating common trade offs between performance power consumption simulation time verification size and cost Details approaches for very low power performances high speed interfaces phase locked loops PLLs voltage controlled oscillators VCOs analog to digital converters ADCs and biomedical filters Delineates the respective parts of a full system on chip SoC from the digital parts to the baseband blocks radio frequency RF circuitries electrostatic discharge ESD structures and built in self test BIST architectures Mixed Signal Circuits explores exciting opportunities in wireless communications and beyond The book is a must for anyone involved in mixed signal circuit design for future technologies <u>Information Technology</u> Ricardo Reis, 2006-04-11 This book contains a selection of tutorials on hot topics in information technology which were presented at the IFIP World Computer Congress WCC2004 took place at the Centre de Congr s Pierre Baudis in Toulouse France from 22 to 27 August 2004 The 11 chapters included in the book were chosen from tutorials proposals submitted to WCC2004 These papers report on several important

and state of the art topics on information technology such as Quality of Service in Information Networks Risk Driven Development of Security Critical Systems Using UMLsec Developing Portable Software Formal Reasoning About Systems Software and Hardware Using Functionals Predicates and Relations The Problematic of Distributed Systems Supervision Software Rejuvenation Modeling and Analysis Test and Design for Test of Mixed Signal Integrated Circuits Web Services Applications of Multi Agent Systems Discrete Event Simulation Human Centered Automation We hereby would like to thank IFIP and more specifically WCC2004 Tutorials Committee and the authors for their contribution We also would like to thank the congress organizers who have done a great job Ricardo Reis Editor QUALITY OF SERVICE IN INFORMATION NETWORKS Augusto Casaca IST INESC R Alves Redol 1000 029 Lisboa Portugal Abstract This article introduces the problems concerned with the provision of end end quality of service in IP networks which are the basis of information networks describes the existing solutions for that provision and presents some of the current research items on the subject Key words Information networks IP networks Integrated Services Differentiated Services Multiprotocol Label Switching UMTS

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Table of Contents Test And Designfortestability In Mixedsignal Integrated

- 1. Understanding the eBook Test And Designfortestability In Mixedsignal Integrated
 - The Rise of Digital Reading Test And Designfortestability In Mixedsignal Integrated
 - o Advantages of eBooks Over Traditional Books
- 2. Identifying Test And Designfortestability In Mixedsignal Integrated
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Test And Designfortestability In Mixedsignal Integrated
 - User-Friendly Interface
- 4. Exploring eBook Recommendations from Test And Designfortestability In Mixedsignal Integrated
 - Personalized Recommendations
 - Test And Designfortestability In Mixedsignal Integrated User Reviews and Ratings
 - Test And Designfortestability In Mixedsignal Integrated and Bestseller Lists
- 5. Accessing Test And Designfortestability In Mixedsignal Integrated Free and Paid eBooks
 - Test And Designfortestability In Mixedsignal Integrated Public Domain eBooks
 - Test And Designfortestability In Mixedsignal Integrated eBook Subscription Services
 - Test And Designfortestability In Mixedsignal Integrated Budget-Friendly Options

- 6. Navigating Test And Designfortestability In Mixedsignal Integrated eBook Formats
 - o ePub, PDF, MOBI, and More
 - Test And Designfortestability In Mixedsignal Integrated Compatibility with Devices
 - Test And Designfortestability In Mixedsignal Integrated Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Test And Designfortestability In Mixedsignal Integrated
 - Highlighting and Note-Taking Test And Designfortestability In Mixedsignal Integrated
 - Interactive Elements Test And Designfortestability In Mixedsignal Integrated
- 8. Staying Engaged with Test And Designfortestability In Mixedsignal Integrated
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Test And Designfortestability In Mixedsignal Integrated
- 9. Balancing eBooks and Physical Books Test And Designfortestability In Mixedsignal Integrated
 - Benefits of a Digital Library
 - o Creating a Diverse Reading Collection Test And Designfortestability In Mixedsignal Integrated
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Test And Designfortestability In Mixedsignal Integrated
 - Setting Reading Goals Test And Designfortestability In Mixedsignal Integrated
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Test And Designfortestability In Mixedsignal Integrated
 - Fact-Checking eBook Content of Test And Designfortestability In Mixedsignal Integrated
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements

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