SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

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Soc Systemonachip Testing For Plug And Play Test Automation

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Soc Systemonachip Testing For Plug And Play Test Automation:

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty,2002-09-30 Various aspects of system on a chip SOC integrated circuit testing are addressed in 13 papers on test planning access and scheduling test data compression and interconnect crosstalk and signal integrity Topics include concurrent test of core based SOC design and testing for interconnect crosstalk defects using on chip embedded processor cores The editor is affiliated with Duke University The book is reprinted from a Special Issue of the Journal of Electronic Testing vol 18 nos 4 5 There is no subject index Annotation c 2003 Book News Inc Portland OR booknews com SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty,2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing *Soc (System-On-a-Chip) Testing for Plug and Play Test Automation* Springer,2014-01-15 **Introduction to Advanced System-on-Chip Test Design and Optimization** Erik Larsson,2006-03-30 SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process Test Resource Partitioning for System-on-a-Chip Vikram Iyengar,Anshuman Chandra,2012-12-06 Test Resource Partitioning for System on a Chip is about test resource partitioning and optimization techniques for plug and play system on a chip SOC test automation Plug and play refers to the paradigm in which core to core interfaces as well as core to SOC logic interfaces are standardized such that cores can be easily plugged into virtual sockets on the SOC design and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator The goal of the book is to position test resource partitioning in the context of SOC test automation as well as to generate interest and

motivate research on this important topic SOC integrated circuits composed of embedded cores are now commonplace Nevertheless There remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols Test Resource Partitioning for System on a Chip responds to a pressing need for a structured methodology for SOC test automation It presents new techniques for the partitioning and optimization of the three major SOC test resources test hardware testing time and test data volume Test Resource Partitioning for System on a Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug and play fashion The framework presented allows the system integrator to reduce test cost and meet short time to market requirements **Reliability, Availability and Serviceability of Networks-on-Chip** Érika Cota,Alexandre de Morais Amory,Marcelo Soares Lubaszewski,2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures **Advances in Electronic Testing** Dimitris Gizopoulos,2006-01-22 Advances in Electronic Testing Challenges and Methodologies is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing The book is a comprehensive elaboration on important topics which capture major research and development efforts today The motivation and inspiration behind this book is to deliver a thorough text that focuses on the evolution of test technology provides insight about the abiding importance of discussed topics records today s state of the art and industrial practices and trends reveals the challenges for emerging testing methodologies and envisages the future of this journey The book consists of eleven edited chapters written by experts in Defect Oriented Testing Nanometer Technologies Failures and Testing Silicon Debug Delay Testing High Speed Test Interfaces DFT Oriented Low Cost Testers Embedded Cores and System on Chip Testing Memory Testing Mixed Signal Testing RF Testing and Loaded Board Testing Contributing authors are affiliated with in alphabetical order Agilent ARM Balearic Islands Univ IBM Inovys Intel LogicVision Magma Mentor Graphics New Mexico Univ Sandia National Labs Synopsys Teradyne and Texas Instruments Advances in Electronic Testing Challenges and Methodologies is an advanced textbook and reference point for senior undergraduate and graduate students in MSc or PhD tracks professors and research leaders in the electronic testing domain It is also for industry design and test engineers and managers seeking a global view and understanding of test technology practices and methodologies and a dense elaboration on test related issues they face in their development projects There is a definite need for documenting the advances in testing I find the work of this edited volume by Dimitris Gizopoulos and his team of authors to be significant and timely the

book provides besidesnovel test methodologies a collective insight into the emerging aspects of testing This I think is beneficial to practicing engineers and researchers both of whom must stay at the forefront of technology This latest addition to the Frontiers Series is destined to serve an important role From the Foreword by Vishwani D Agrawal Consulting Editor Frontiers in Electronic Testing Book Series **Oscillation-Based Test in Mixed-Signal Circuits** Gloria Huertas Sánchez,Diego Vázquez García de la Vega,Adoración Rueda Rueda,Jose Luis Huertas Díaz,2007-06-03 Oscillation Based Test in Mixed Signal Circuits presents the development and experimental validation of the structural test strategy called Oscillation Based Test OBT in short The results here presented allow to assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits The Core Test Wrapper Handbook Francisco da Silva,Teresa McLaurin,Tom Waayers,2006-09-15 In the early to mid 1990 s while working at what was then Motorola Se conductor business changes forced my multi hundred dollar microprocessor to become a tens of dollars embedded core I ran into first hand the problem of trying to deliver what used to be a whole chip with something on the order of over 400 interconnect signals to a design team that was going to stuff it into a package with less than 220 signal pins and surround it with other logic I also ran into the problem of delivering microprocessor specification verifi tion a microprocessor is not just about the functions and instructions included with the instruction set but also the MIPs rating at some given f quency I faced two dilemmas one I could not deliver functional vectors without significant development of off core logic to deal with the reduced chip I O map and everybody s I O map was going to be a little different and two the JTAG 1149 1 boundary scan ring that was around my core when it was a chip was going to be woefully inadequate since it did not support speed signal application and capture and independent use separate from my core I considered the problem at length and came up with my own solution that was predominantly a separate non JTAG scan test wrapper that supported at speed application of launch capture cycles using the system clock But my problems weren t over at that point either **Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits** Manoj Sachdev,José Pineda de Gyvez,2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are

applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent

New Methods of Concurrent Checking Michael Gössel,Vitaly Ocheretny,Egor Sogomonyan,Daniel Marienfeld,2008-04-26 Computers are everywhere around us We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation Computers are incredibly fast inexpensive and equipped with almost unimag able large storage capacity Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the world can be 2 easily accommodated on an ordinary chip The size of such a chip is less than 1 cm This is a fantastic achievement for an unbelievably low price However the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future Can we always trust computers Are computers always reliable Are chips suf ciently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by c current checking Besides permanent faults many temporary or transient faults are also to be expected Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation Alfredo Benso,Paolo Prinetto,2005-12-15 Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation intends to be a comprehensive guide to Fault Injection techniques used to evaluate the dependability of a digital system The description and the critical analysis of different Fault Injection techniques and tools will be authored by key scientists in the field of system dependability and fault tolerance *Digital Timing Measurements* Wolfgang Maichen,2006-10-03 As many circuits and applications now enter the Gigahertz frequency range accurate digital timing measurements have become crucial in the design verification characterization and application of electronic circuits To be successful in this endeavour an engineer needs a knowledge base covering instrumentation measurement techniques signal integrity jitter and timing concepts and statistics Very often even the most experienced digital test engineers while mastering some of those subjects lack systematic knowledge or experience in the high speed signal area Digital Timing Measurements gives a compact practice oriented overview on all those subjects The emphasis is on useable concepts and real life guidelines that can be readily put into practice with references to the underlying mathematical theory It unites in one place a variety of information relevant to high speed testing measurement signal fidelity and instrumentation Fault-Tolerance Techniques for SRAM-Based FPGAs Fernanda Lima Kastensmidt,Ricardo Reis,2007-02-01 Fault tolerance in integrated circuits is not an exclusive concern regarding space designers or highly reliable application engineers Rather designers of next generation products must cope with reduced margin noises due to technological advances The continuous evolution of the fabrication

technology process of semiconductor components in terms of transistor geometry shrinking power supply speed and logic density has significantly reduced the reliability of very deep submicron integrated circuits in face of the various internal and external sources of noise The very popular Field Programmable Gate Arrays customizable by SRAM cells are a consequence of the integrated circuit evolution with millions of memory cells to implement the logic embedded memories routing and more recently with embedded microprocessors cores These re programmable systems on chip platforms must be fault tolerant to cope with present days requirements This book discusses fault tolerance techniques for SRAM based Field Programmable Gate Arrays FPGAs It starts by showing the model of the problem and the upset effects in the programmable architecture In the sequence it shows the main fault tolerance techniques used nowadays to protect integrated circuits against errors A large set of methods for designing fault tolerance systems in SRAM based FPGAs is described Some presented techniques are based on developing a new fault tolerant architecture with new robustness FPGA elements Other techniques are based on protecting the high level hardware description before the synthesis in the FPGA The reader has the flexibility of choosing the most suitable fault tolerance technique for its project and to compare a set of fault tolerant techniques for programmable logic applications **Embedded Processor-Based Self-Test** Dimitris Gizopoulos,A. Paschalis,Yervant Zorian,2013-03-09 Embedded Processor Based Self Test is a guide to self testing strategies for embedded processors Embedded processors are regularly used today in most System on Chips SoCs Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them This is due to the complex sequential structure of processor architectures which consists of high performance datapath units and sophisticated control logic for performance optimization Structured Design for Testability DfT and hardware based self testing techniques which usually have a non trivial impact on a circuit s performance size and power can not be applied without serious consideration and careful incorporation into the processor design Embedded Processor Based Self Test shows how the powerful embedded functionality that processors offer can be utilized as a self testing resource Through a discussion of different strategies the book emphasizes on the emerging area of Software Based Self Testing SBST SBST is based on the idea of execution of embedded software programs to perform self testing of the processor itself and its surrounding blocks in the SoC SBST is a low cost strategy in terms of overhead area speed power development effort and test application cost as it is applied using low cost low speed test equipment Embedded Processor Based Self Test can be used by designers DfT engineers test practitioners researchers and students working on digital testing and in particular processor and SoC test This book sets the framework for comparisons among different SBST methodologies by discussing key requirements It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures **Testing Static Random Access Memories** Said Hamdioui,2013-06-29 Testing Static Random Access Memories covers testing of one of the important semiconductor memories types it addresses testing of static

random access memories SRAMs both single port and multi port It contributes to the technical acknowledge needed by those involved in memory testing engineers and researchers The book begins with outlining the most popular SRAMs architectures Then the description of realistic fault models based on defect injection and SPICE simulation are introduced Thereafter high quality and low cost test patterns as well as test strategies for single port two port and any p port SRAMs are presented together with some preliminary test results showing the importance of the new tests in reducing DPM level The impact of the port restrictions e g read only ports on the fault models tests and test strategies is also discussed Features Fault primitive based analysis of memory faults A complete framework of and classification memory faults A systematic way to develop optimal and high quality memory test algorithms A systematic way to develop test patterns for any multi port SRAM Challenges and trends in embedded memory testing **High Performance Memory Testing** R. Dean Adams,2005-12-29 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author s 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested **Power-Constrained Testing of VLSI Circuits** Nicola Nicolici,Bashir M. Al-Hashimi,2006-04-11 This text focuses on techniques for minimizing power dissipation during test application at logic and register transfer levels of abstraction of the VLSI design flow It surveys existing techniques and presents several test automation techniques for reducing power in scan based sequential circuits and BIST data paths **Verification by Error Modeling** Katarzyna Radecka,Zeljko Zilic,2005-12-17 1 DESIGN FLOW Integrated circuit IC complexity is steadily increasing ICs incorporating hundreds of millions of transistors mega bit memories complicated pipelined structures etc are now in high demand For example Intel Itanium II processor contains more than 200 million transistors including a 3 MB third level cache A billion transistor IC was said to be imminently doable by Intel fellow J Crawford at Microprocessor Forum in October 2002 40 Obviously designing such complex circuits poses real challenges to engineers Certainly no relief comes from the competitive marketplace with increasing demands for a very narrow window of time time to market in engineering a ready product Therefore a systematic and well structured approach to designing ICs is a must Although there are no widely adhered standards for a design flow most companies have their own established practices which they follow closely for in house design processes In general however a typical product cycle includes few milestones An idea for a new product starts usually from an depth market analysis of customer needs Once a window of opportunity is found product requirements are carefully specified Ideally these parameters would not change during the design process In practice initial phases of preparing a

design specification are susceptible to potential errors as it is very difficult to grasp all the details in a complex design

Data Mining and Diagnosing IC Fails Leendert M. Huisman,2006-10-03 This book grew out of an attempt to describe a variety of tools that were developed over a period of years in IBM to analyze Integrated Circuit fail data The selection presented in this book focuses on those tools that have a significant statistical or datamining component The danger of describing sta tistical analysis methods is the amount of non trivial mathematics that is involved and that tends to obscure the usually straigthforward analysis ideas This book is therefore divided into two roughly equal parts The first part contains the description of the various analysis techniques and focuses on ideas and experimental results The second part contains all the mathematical details that are necessary to prove the validity of the analysis techniques the existence of solutions to the problems that those techniques engender and the correctness of several properties that were assumed in the first part Those who are interested only in using the analysis techniques themselves can skip the second part but that part is important if only to understand what is being done

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Table of Contents Soc Systemonachip Testing For Plug And Play Test Automation

1. Understanding the eBook Soc Systemonachip Testing For Plug And Play Test Automation
    - The Rise of Digital Reading Soc Systemonachip Testing For Plug And Play Test Automation
    - Advantages of eBooks Over Traditional Books
2. Identifying Soc Systemonachip Testing For Plug And Play Test Automation
    - Exploring Different Genres
    - Considering Fiction vs. Non-Fiction
    - Determining Your Reading Goals
3. Choosing the Right eBook Platform
    - Popular eBook Platforms
    - Features to Look for in an Soc Systemonachip Testing For Plug And Play Test Automation
    - User-Friendly Interface

4. Exploring eBook Recommendations from Soc Systemonachip Testing For Plug And Play Test Automation
    - Personalized Recommendations
    - Soc Systemonachip Testing For Plug And Play Test Automation User Reviews and Ratings
    - Soc Systemonachip Testing For Plug And Play Test Automation and Bestseller Lists
5. Accessing Soc Systemonachip Testing For Plug And Play Test Automation Free and Paid eBooks
    - Soc Systemonachip Testing For Plug And Play Test Automation Public Domain eBooks
    - Soc Systemonachip Testing For Plug And Play Test Automation eBook Subscription Services
    - Soc Systemonachip Testing For Plug And Play Test Automation Budget-Friendly Options
6. Navigating Soc Systemonachip Testing For Plug And Play Test Automation eBook Formats
    - ePub, PDF, MOBI, and More
    - Soc Systemonachip Testing For Plug And Play Test Automation Compatibility with Devices
    - Soc Systemonachip Testing For Plug And Play Test Automation Enhanced eBook Features
7. Enhancing Your Reading Experience
    - Adjustable Fonts and Text Sizes of Soc Systemonachip Testing For Plug And Play Test Automation
    - Highlighting and Note-Taking Soc Systemonachip Testing For Plug And Play Test Automation
    - Interactive Elements Soc Systemonachip Testing For Plug And Play Test Automation
8. Staying Engaged with Soc Systemonachip Testing For Plug And Play Test Automation
    - Joining Online Reading Communities
    - Participating in Virtual Book Clubs
    - Following Authors and Publishers Soc Systemonachip Testing For Plug And Play Test Automation
9. Balancing eBooks and Physical Books Soc Systemonachip Testing For Plug And Play Test Automation
    - Benefits of a Digital Library
    - Creating a Diverse Reading Collection Soc Systemonachip Testing For Plug And Play Test Automation
10. Overcoming Reading Challenges
    - Dealing with Digital Eye Strain
    - Minimizing Distractions
    - Managing Screen Time
11. Cultivating a Reading Routine Soc Systemonachip Testing For Plug And Play Test Automation
    - Setting Reading Goals Soc Systemonachip Testing For Plug And Play Test Automation
    - Carving Out Dedicated Reading Time

12. Sourcing Reliable Information of Soc Systemonachip Testing For Plug And Play Test Automation
    - Fact-Checking eBook Content of Soc Systemonachip Testing For Plug And Play Test Automation
    - Distinguishing Credible Sources
13. Promoting Lifelong Learning
    - Utilizing eBooks for Skill Development
    - Exploring Educational eBooks
14. Embracing eBook Trends
    - Integration of Multimedia Elements
    - Interactive and Gamified eBooks

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