

Static
Random-Access
Memory (SRAM)



Integrated
Circuit
Technology



Testing Static Random Access Memories

Manoj Sachdev, José Pineda de Gyvez



Testing Static Random Access Memories:

Testing Static Random Access Memories Said Hamdioui, 2004-03-31 Embedded memories are one of the fastest growing segments of today's new technology market. According to the 2001 International Technology Roadmap for Semiconductors, embedded memories will continue to dominate the increasing system on chip SoC content in the next several years, approaching 94% of the SoC area in about 10 years. Furthermore, the shrinking size of manufacturing structures makes memories more sensitive to defects. Consequently, the memory yield will have a dramatic impact on the overall Defect per million level, hence on the overall SoC yield. Meeting a high memory yield requires understanding memory designs, modeling their faulty behaviors, designing adequate tests and diagnosis algorithms, as well as efficient self-test and repair schemes. Testing Static Random Access Memories covers testing of one of the important semiconductor memory types: it addresses testing of static random access memories (SRAMs), both single port and multi port. It contributes to the technical knowledge needed by those involved in memory testing: engineers and researchers. The book begins with outlining the most popular SRAM architectures. Then, the description of realistic fault models based on defect injection and SPICE simulation are introduced. Thereafter, high quality and low cost test patterns, as well as test strategies for single port, two port, and any p port SRAMs, are presented together with some preliminary test results showing the importance of the new tests in reducing DPM level. The impact of the port restrictions, e.g., read only ports on the fault models, tests, and test strategies is also discussed.

High Performance Memory Testing R. Dean Adams, 2005-12-29 Are memory applications more critical than they have been in the past? Yes, but even more critical is the number of designs and the sheer number of bits on each design. It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully. High Performance Memory Testing: Design Principles, Fault Modeling, and Self Test is based on the author's 20 years of experience in memory design, memory reliability development, and memory self test. High Performance Memory Testing: Design Principles, Fault Modeling, and Self Test is written for the professional and the researcher to help them understand the memories that are being tested. Advanced Test Methods for SRAMs Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, 2009-10-08

Modern electronics depend on nanoscaled technologies that present new challenges in terms of testing and diagnostics. Memories are particularly prone to defects since they exploit the technology limits to get the highest density. This book is an invaluable guide to the testing and diagnostics of the latest generation of SRAM, one of the most widely applied types of memory. Classical methods for testing memory are designed to handle the so-called static faults, but these test solutions are not sufficient for faults that are emerging in the latest Very Deep Sub Micron VDSM technologies. These new fault models, referred to as dynamic faults, are not covered by classical test solutions and require the dedicated test sequences presented in this book. **Digital Logic**

Testing and Simulation Alexander Miczo, 2003-10-10 Your road map for meeting today's digital testing challenges. Today

digital logic devices are common in products that impact public safety including applications in transportation and human implants. Accurate testing has become more critical to reliability safety and the bottom line. Yet as digital systems become more ubiquitous and complex the challenge of testing them has become more difficult. As one development group designing a RISC stated the work required to test a chip of this size approached the amount of effort required to design it. A valued reference for nearly two decades *Digital Logic Testing and Simulation* has been significantly revised and updated for designers and test engineers who must meet this challenge. There is no single solution to the testing problem. Organized in an easy to follow sequential format this Second Edition familiarizes the reader with the many different strategies for testing and their applications and assesses the strengths and weaknesses of the various approaches. The book reviews the building blocks of a successful testing strategy and guides the reader on choosing the best solution for a particular application. *Digital Logic Testing and Simulation Second Edition* covers such key topics as Binary Decision Diagrams BDDs and cycle based simulation Tester architectures Standard Test Interface Language STIL Practical algorithms written in a Hardware Design Language HDL Fault tolerance Behavioral Automatic Test Pattern Generation ATPG The development of the Test Design Expert TDX the many obstacles encountered and lessons learned in creating this novel testing approach Up to date and comprehensive *Digital Logic Testing and Simulation* is an important resource for anyone charged with pinpointing faulty products and assuring quality safety and profitability

Mathematical and Engineering Methods in Computer Science Antonin Kucera, Thomas A. Henzinger, Jaroslav Nešetřil, Tomas Vojnar, David Antos, 2013-01-17 This volume contains the post proceedings of the 8th Doctoral Workshop on Mathematical and Engineering Methods in Computer Science MEMICS 2012 held in Znojmo Czech Republic in October 2012. The 13 thoroughly revised papers were carefully selected out of 31 submissions and are presented together with 6 invited papers. The topics covered by the papers include computer aided analysis and verification applications of game theory in computer science networks and security modern trends of graph theory in computer science electronic systems design and testing and quantum information processing

VLSI Test Principles and Architectures Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume. Most up to date coverage of design for testability. Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

Digital Timing Measurements Wolfgang Maichen, 2006-10-03 As many circuits and applications now enter the Gigahertz frequency range accurate digital timing measurements have become crucial in the design verification characterization and application of electronic circuits. To be successful in this endeavour an engineer needs a knowledge base covering instrumentation measurement techniques signal integrity jitter and timing concepts and statistics. Very often even the most experienced

digital test engineers while mastering some of those subjects lack systematic knowledge or experience in the high speed signal area Digital Timing Measurements gives a compact practice oriented overview on all those subjects The emphasis is on useable concepts and real life guidelines that can be readily put into practice with references to the underlying mathematical theory It unites in one place a variety of information relevant to high speed testing measurement signal fidelity and instrumentation

Emerging Nanotechnologies Mohammad Tehranipoor, 2007-12-08 Emerging Nanotechnologies Test Defect Tolerance and Reliability covers various technologies that have been developing over the last decades such as chemically assembled electronic nanotechnology Quantum dot Cellular Automata QCA and nanowires and carbon nanotubes Each of these technologies offers various advantages and disadvantages Some suffer from high power some work in very low temperatures and some others need indeterministic bottom up assembly These emerging technologies are not considered as a direct replacement for CMOS technology and may require a completely new architecture to achieve their functionality Emerging Nanotechnologies Test Defect Tolerance and Reliability brings all of these issues together in one place for readers and researchers who are interested in this rapidly changing field

New Methods of Concurrent Checking Michael Gössel, Vitaly Ocheretny, Egor Sogomonyan, Daniel Marienfeld, 2008-04-26 Computers are everywhere around us We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation Computers are incredibly fast inexpensive and equipped with almost unimaginable large storage capacity Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the world can be easily accommodated on an ordinary chip The size of such a chip is less than 1 cm This is a fantastic achievement for an unbelievably low price However the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future Can we always trust computers Are computers always reliable Are chips sufficiently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by current checking Besides permanent faults many temporary or transient faults are also to be expected

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC

VLSI circuits testing is an activity associated with every level of integration. However, special emphasis is placed on wafer level test and final test. Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted. Basic digital tests are applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well. Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing, DDQ, stuck at testing, low voltage testing, etc. This partitioning choice is actually application dependent.

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Table of Contents Testing Static Random Access Memories

1. Understanding the eBook Testing Static Random Access Memories
 - The Rise of Digital Reading Testing Static Random Access Memories
 - Advantages of eBooks Over Traditional Books
2. Identifying Testing Static Random Access Memories
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Testing Static Random Access Memories
 - User-Friendly Interface
4. Exploring eBook Recommendations from Testing Static Random Access Memories
 - Personalized Recommendations
 - Testing Static Random Access Memories User Reviews and Ratings
 - Testing Static Random Access Memories and Bestseller Lists
5. Accessing Testing Static Random Access Memories Free and Paid eBooks
 - Testing Static Random Access Memories Public Domain eBooks
 - Testing Static Random Access Memories eBook Subscription Services
 - Testing Static Random Access Memories Budget-Friendly Options

6. Navigating Testing Static Random Access Memories eBook Formats
 - ePub, PDF, MOBI, and More
 - Testing Static Random Access Memories Compatibility with Devices
 - Testing Static Random Access Memories Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Testing Static Random Access Memories
 - Highlighting and Note-Taking Testing Static Random Access Memories
 - Interactive Elements Testing Static Random Access Memories
8. Staying Engaged with Testing Static Random Access Memories
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Testing Static Random Access Memories
9. Balancing eBooks and Physical Books Testing Static Random Access Memories
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Testing Static Random Access Memories
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Testing Static Random Access Memories
 - Setting Reading Goals Testing Static Random Access Memories
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Testing Static Random Access Memories
 - Fact-Checking eBook Content of Testing Static Random Access Memories
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements

- Interactive and Gamified eBooks

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