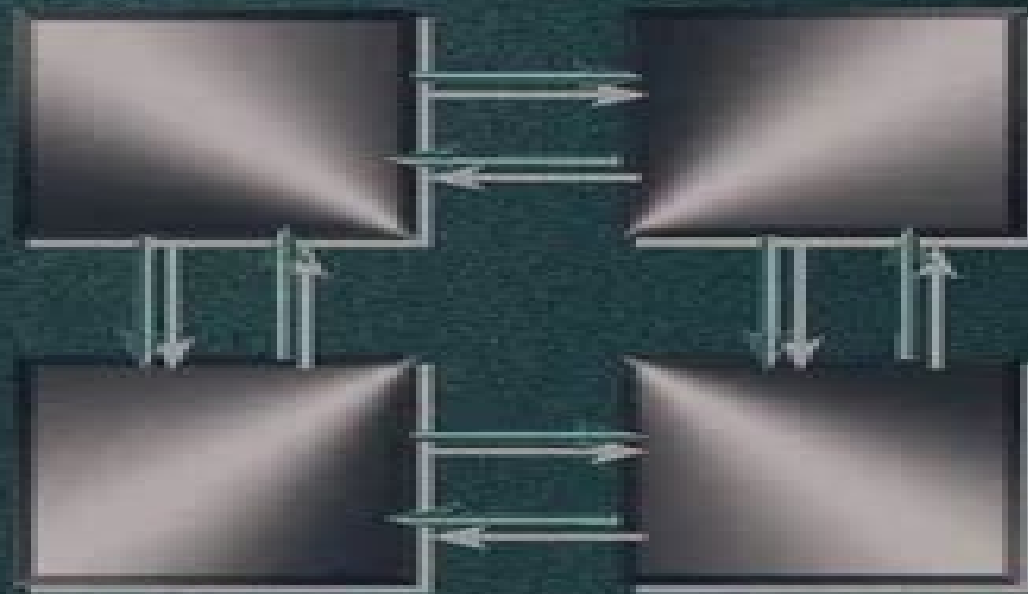


Specification and Verification of Systolic Arrays



Nam Ling & Magdy A Bayoumi

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Specification And Verification Of Systolic Arrays Magdy A Bayoumi, Nam Ling, 1999-08-05 Circuits and architectures have become more complex in terms of structure interconnection topology and data flow Design correctness has become increasingly significant as errors in design may result in strenuous debugging or even in the repetition of a costly manufacturing process Although circuit simulation has been used traditionally and widely as the technique for checking hardware and architectural designs it does not guarantee the conformity of designs to specifications Formal methods therefore become vital in guaranteeing the correctness of designs and have thus received a significant amount of attention in the CAD industry today This book presents a formal method for specifying and verifying the correctness of systolic array designs Such architectures are commonly found in the form of accelerators for digital signal image and video processing These arrays can be quite complicated in topology and data flow In the book a formalism called STA is defined for these kinds of dynamic environments with a survey of related techniques A framework for specification and verification is established Formal verification techniques to check the correctness of the systolic networks with respect to the algorithmic level specifications are explained The book also presents a Prolog based formal design verifier named VSTA developed to automate the verification process as using a general purpose theorem prover is usually extremely time consuming Several application examples are included in the book to illustrate how formal techniques and the verifier can be used to automate proofs

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Berra,1993-08-16 This three volume work presents a compendium of current and seminal papers on parallel distributed processing offered at the 22nd International Conference on Parallel Processing held August 16 20 1993 in Chicago Illinois Topics include processor architectures mapping algorithms to parallel systems performance evaluations fault diagnosis recovery and tolerance cube networks portable software synchronization compilers hypercube computing and image processing and graphics Computer professionals in parallel processing distributed systems and software engineering will find this book essential to their complete computer reference library Algorithm Engineering for Integral and Dynamic Problems Lucia Rapanotti,2001-01-23 Algorithm engineering allows computer engineers to produce a computational machine that will execute an algorithm as efficiently and cost effectively as possible given a set of constraints such as minimal performance or the availability of technology Addressing algorithm engineering in a parallel setting regular array syntheses offer powerful computation and embody best practice but often face the criticism that they are applicable only to restricted classes of algorithms Algorithm Engineering for Integral and Dynamic Problems reviews the basic principles of regular array synthesis and shows how to extend its use into classes of algorithms traditionally viewed to be beyond its domain of application The author discusses the transformation of the initial algorithm specification into a specification with data dependencies of increased regularity in order to obtain corresponding regular arrays by direct application of the standard mapping techniques The book includes a review of the basic principles of regular array synthesis followed by applications of these techniques to well known algorithms concluding with numerous case studies to illustrate the methods Researchers and practitioners in algorithm engineering will find that this text significantly extends their understanding of the applications of regular array synthesis and regular array processors beyond the traditionally narrow field of relevance **PARLE '92, Parallel Architectures and Languages Europe** Daniel Etiemble,1992-06-03 The 1992 Parallel Architectures and Languages Europe conference continues the tradition of a wide and representative international meeting of specialists from academia and industry in theory design and application of parallel computer systems set by the previous PARLE conferences held in Eindhoven in 1987 1989 and 1991 This volume contains the 52 regular and 25 poster papers that were selected from 187 submitted papers for presentation and publication In addition five invited lectures are included The regular papers are organized into sections on implementation of parallel programs graph theory architecture optimal algorithms graph theory and performance parallel software components data base optimization and modeling data parallelism formal methods systolic approach functional programming fine grain parallelism Prolog data flow systems network efficiency parallel algorithms cache systems implementation of parallel languages parallel scheduling in data base systems semantic models parallel data base machines and language semantics **Computer Hardware Description Languages and their Applications** D. Agnew,L. Claesen,R. Camposano,2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by

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