SOFTWARE SYNTHESIS FROM DATAFLOW GRAPHS

Edited by:

Jonathan Allen

Software Synthesis From Dataflow Graphs

Shuvra S. Bhattacharyya,Praveen K. Murthy,Edward A. Lee

Software Synthesis From Dataflow Graphs:

Software Synthesis from Dataflow Graphs Shuvra S. Bhattacharyya,Praveen K. Murthy,Edward A. Lee,1996-05-31 Software Synthesis from Dataflow Graphs addresses the problem of generating efficient software implementations from applications specified as synchronous dataflow graphs for programmable digital signal processors DSPs used in embedded real time systems The advent of high speed graphics workstations has made feasible the use of graphical block diagram programming environments by designers of signal processing systems A particular subset of dataflow called Synchronous Dataflow SDF has proven efficient for representing a wide class of unirate and multirate signal processing algorithms and has been used as the basis for numerous DSP block diagram based programming environments such as the Signal Processing Workstation from Cadence Design Systems Inc COSSAP from Synopsys both commercial tools and the Ptolemy environment from the University of California at Berkeley A key property of the SDF model is that static schedules can be determined at compile time This removes the overhead of dynamic scheduling and is thus useful for real time DSP programs where throughput requirements are often severe Another constraint that programmable DSPs for embedded systems have is the limited amount of on chip memory Off chip memory is not only expensive but is also slower and increases the power consumption of the system hence it is imperative that programs fit in the on chip memory whenever possible Software Synthesis from Dataflow Graphs reviews the state of the art in constructing static memory optimal schedules for programs expressed as SDF graphs Code size reduction is obtained by the careful organization of loops in the target code Data buffering is optimized by constructing the loop hierarchy in provably optimal ways for many classes of SDF graphs The central result is a uniprocessor scheduling framework that provably synthesizes the most compact looping structures called single appearance schedules for a certain class of SDF graphs In addition algorithms and heuristics are presented that generate single appearance schedules optimized for data buffering usage Numerous practical examples and extensive experimental data are provided to illustrate the efficacy of these techniques *Software Synthesis from Dataflow Graphs* Shuvra S. Bhattacharyya,Praveen K. Murthy,Edward A. Lee,2012-12-06 Software Synthesis from Dataflow Graphs addresses the problem of generating efficient software implementations from applications specified as synchronous dataflow graphs for programmable digital signal processors DSPs used in embedded real time systems The advent of high speed graphics workstations has made feasible the use of graphical block diagram programming environments by designers of signal processing systems A particular subset of dataflow called Synchronous Dataflow SDF has proven efficient for representing a wide class of unirate and multirate signal processing algorithms and has been used as the basis for numerous DSP block diagram based programming environments such as the Signal Processing Workstation from Cadence Design Systems Inc COSSAP from Synopsys both commercial tools and the Ptolemy environment from the University of California at Berkeley A key property of the SDF model is that static schedules can be determined at compile time This removes the overhead of

dynamic scheduling and is thus useful for real time DSP programs where throughput requirements are often severe Another constraint that programmable DSPs for embedded systems have is the limited amount of on chip memory Off chip memory is not only expensive but is also slower and increases the power consumption of the system hence it is imperative that programs fit in the on chip memory whenever possible Software Synthesis from Dataflow Graphs reviews the state of the art in constructing static memory optimal schedules for programs expressed as SDF graphs Code size reduction is obtained by the careful organization of loops in the target code Data buffering is optimized by constructing the loop hierarchy in provably optimal ways for many classes of SDF graphs The central result is a uniprocessor scheduling framework that provably synthesizes the most compact looping structures called singleappearance schedules for a certain class of SDF graphs In addition algorithms and heuristics are presented that generate single appearance schedules optimized for data buffering usage Numerous practical examples and extensive experimental data are provided to illustrate the efficacy of these techniques Handbook of Signal Processing Systems Shuvra S. Bhattacharyya,Ed F. Deprettere,Rainer Leupers,Jarmo Takala,2013-06-20 Handbook of Signal Processing Systems is organized in three parts The first part motivates representative applications that drive and apply state of the art methods for design and implementation of signal processing systems the second part discusses architectures for implementing these applications the third part focuses on compilers and simulation tools describes models of computation and their associated design tools and methodologies This handbook is an essential tool for professionals in many fields and researchers of all levels **Field-Programmable Logic and Applications: The Roadmap to Reconfigurable Computing** Reiner W. Hartenstein,Herbert Grünbacher,2003-06-29 This book is the proceedings volume of the 10th International Conference on Field Programmable Logic and its Applications FPL held August 27 30 2000 in Villach Austria which covered areas like reconfigurable logic RL reconfigurable computing RC and its applications and all other aspects Its subtitle The Roadmap to Reconfigurable Computing reminds us that we are currently witnessing the runaway of a breakthrough The annual FPL series is the eldest international conference in the world covering configware and all its aspects It was founded 1991 at Oxford University UK and is 2 years older than its two most important competitors usually taking place at Monterey and Napa FPL has been held at Oxford Vienna Prague Darmstadt London Tallinn and Glasgow also see http www fpl uni kl de FPL The New Case for Reconfigurable Platforms Converging Media Indicated by palmtops smart mobile phones many other portables and consumer electronics media such as voice sound video TV wireless cable telephone and Internet continue to converge This creates new opportunities and even necessities for reconfigurable platform usage The new converged media require high volume flexible multi purpose multi standard low power products adaptable to support evolving standards emerging new standards field upgrades bug fixes and to meet the needs of a growing number of different kinds of services offered to zillions of individual subscribers preferring different media mixes **Software and Compilers for Embedded Systems** Henk Schepers,2004-10-29 This volume contains the

proceedings of the 8th International Workshop on Software and Compilers for Embedded Systems SCOPES 2004 held in A terdam The Netherlands on September 2 and 3 2004 Initially the workshop was referred to as the International Workshop on Code Generation for Emb ded Systems The rst took place in 1994 in Schlo Dagstuhl Germany From its beginnings the intention of the organizers has been to create an interactive atmosphere in which the participants can discuss and pro t from the assembly of international experts in the eld The name SCOPES has been used since the fourth edition in St Goar G many in1999whenthescopeoftheworkshopwasextendedtoalsocovergeneral issues in embedded software design Since then SCOPES has been held again in St Goar in 2001 Berlin Germany in 2002 Vienna Austria in 2003 and now in Amsterdam The Netherlands In response to the call for papers almost 50 very strong papers were s mitted from all over the world All submitted papers were reviewed by at least three experts to ensure the quality of the workshop In the end the program committee selected 17 papers for presentation at the workshop These papers are divided into the following categories application speci c co design system and application synthesis data ow analysis data partitioning task scheduling and code generation In addition to the selected contributions the keynote address was delivered by Mike Uhler from MIPS Technologies An abstract of his talk is also included in this volume **ECOOP 2008 - Object-Oriented Programming** Jan Vitek,2008-07-01 It is a pleasure to present the proceedings of the 22nd European Conference on Object Oriented Programming ECOOP 2008 held in Paphos Cyprus The conference continues to serve a broad object oriented community with a tech cal program spanning theory and practice and a healthy mix of industrial and academic participants This year a strong workshop and tutorial program c plementedthemaintechnicaltrack Wehad13workshopsand8tutorials aswell as the co located Dynamic Language Symposium DLS Finally the program was rounded out with a keynote by Rachid Guerraoui and a banquet speech by James Noble As in previous years two Dahl Nygaard awards were selected by AITO and for the rst time the ECOOP Program Committee gave a best paper award Theproceedingsinclude27papersselectedfrom138submissions Thepapers werereviewed in a single blind process with three to ve reviews per paper P liminaryversionsofthereviewsweremadeavailabletotheauthorsaweekbefore the PC meeting to allow for short 500 words or less author responses The sponses were discussed at the PC meeting and were instrumental in reaching decisions The PC discussions followed Oscar Nierstrasz Champion pattern PC papers had ve reviews and were held at a higher standard **Distributed Embedded Systems: Design, Middleware and Resources** Bernd Kleinjohann,Lisa Kleinjohann,Marilyn Wolf,2008-07-10 This year the IFIP Working Conference on Distributed and Parallel Embedded Sys tems DIPES 2008 is held as part of the IFIP World Computer Congress held in Milan on September 7 10 2008 The embedded systems world has a great deal of experience with parallel and distributed computing Many embedded computing systems require the high performance that can be delivered by parallel computing Parallel and distributed computing are often the only ways to deliver adequate real time performance at low power levels This year s conference attracted 30 submissions of which 21

were accepted Prof Jor g Henkel of the University of Karlsruhe graciously contributed a keynote address on embedded computing and reliability We would like to thank all of the program committee members for their diligence Wayne Wolf Bernd Kleinjohann and Lisa Kleinjohann Acknowledgements We would like to thank all people involved in the organization of the IFIP World Computer Congress 2008 especially the IPC Co Chairs Judith Bishop and Ivo De Lotto the Organization Chair Giulio Occhini as well as the Publications Chair John Impagliazzo Further thanks go to the authors for their valuable contributions to DIPES 2008 Last but not least we would like to acknowledge the considerable amount of work and enthusiasm spent by our colleague Claudius Stern in preparing theproceedingsofDIPES2008 Hemadeitpossibletoproducethemintheircurrent professional and homogeneous style   Embedded Systems Handbook Richard Zurawski,2018-09-03 Considered a standard industry resource the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications including those in automotive electronics industrial automated systems and building automation and control Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again Divided into two volumes to accommodate this growth the Embedded Systems Handbook Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews that explore cutting edge developments and deployments and identify potential trends This first self contained volume of the handbook Embedded Systems Design and Verification is divided into three sections It begins with a brief introduction to embedded systems design and verification It then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Those interested in taking their work with embedded systems to the network level should complete their study with the second volume Network Embedded Systems   **Embedded Systems Handbook 2-Volume Set** Richard Zurawski,2018-10-08 During the past few years there has been an dramatic upsurge in research and development implementations of new technologies and deployments of actual solutions and technologies in the diverse application areas of embedded systems These areas include automotive electronics industrial automated systems and building automation and control Comprising 48 chapters and the contributions of 74 leading experts from industry and academia the Embedded Systems Handbook Second Edition presents a comprehensive view of embedded systems their design verification networking and applications The contributors directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews exploring new developments deployments and trends To accommodate the tremendous growth in the field the handbook is now divided into two volumes

New in This Edition Processors for embedded systems Processor centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections It begins with a brief introduction to embedded systems design and verification The book then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Networked Embedded Systems Volume II focuses on selected application areas of networked embedded systems It covers automotive field industrial automation building automation and wireless sensor networks This volume highlights implementations in fast evolving areas which have not received proper coverage in other publications Reflecting the unique functional requirements of different application areas the contributors discuss inter node communication aspects in the context of specific applications of networked embedded systems **Model Based System Engineering** Ali Koudri,2025-09-10 Well structured and interdisciplinary overview of MBSE covering both theoretical foundations and practical applications Taking an interdisciplinary approach Model Based System Engineering provides a comprehensive introduction to understanding and applying model based system engineering MBSE principles and practices in the design development and management of complex systems Throughout the book readers will find case studies practical examples and exercises and multiple choice questions that reinforce key concepts and promote active learning The book begins by exploring the historical context of MBSE highlighting its emergence as a response to the limitations of traditional document centric approaches It emphasizes the crucial role of abstraction in MBSE and introduces key concepts definitions and taxonomies that form the bedrock of this discipline Subsequent chapters delve into the core principles of modeling examining the intricate relationships between systems languages and models Sample topics covered in Model Based System Engineering include Prefaced by Bran Selic a world authority on MBSE and software engineering Model verification and validation exploring various techniques such as model checking simulation and testing that enable the early detection and resolution of design errors and inconsistencies Model based system architecting methodological considerations and application in real world contexts Various modeling paradigms including structural and behavioral models The pivotal role of languages in enabling effective modeling practices Benefits of formalization in enhancing the precision consistency and analyzability of system models Model Based System Engineering is an essential resource for systems engineers researchers and students seeking to understand and harness the power of MBSE in tackling the complexities of modern systems Component-Based Software Development for Embedded Systems Colin Atkinson,Christian Bunse,Hans-Gerhard Gross,Christian Peper,2005-11-19 Embedded systems are ubiquitous They appear in cell phones microwave ovens refrigerators consumer electronics cars and jets Some of these embedded s tems are safety or security critical such as in medical equipment nuclear plants and X by wire control systems in naval

ground and aerospace transportation hicles With the continuing shift from hardware to software embedded systems are increasingly dominated by embedded software Embedded software is complex Its engineering inherently involves a mul disciplinary interplay with the physics of the embedding system or environment Embedded software also comes in ever larger quantity and diversity The next generation of premium automobiles will carry around one gigabyte of binary code The proposed US DDX submarine is e ectively a oating embedded so ware system comprising 30 billion lines of code written in over 100 programming languages Embedded software is expensive Cost estimates are quoted at around US 15 30 per line from commencement to shipping In the defense realm costs can range up to 100 while for highly critical applications such as the Space Shuttle the cost per line approximates 1 000 In view of the exponential increase in complexity the projected costs of future embedded software are staggering **Readings in Hardware/Software Co-Design** Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction ans reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s *Specification and Design Methodology for Real-Time Embedded Systems* Randall S. Janka,2012-12-06 Specification and design methodology has seen significant growth as a research area over the last decade tracking but lagging behind VLSI design technology in general and the CAD industry in particular The commercial rush to market tries to leverage existing technology which fuels CAD design tool development Paralleling this is very active basic and applied research to investigate and move forward rational and effective methodologies for accomplishing digital design especially in the field of hardware software codesign It is this close relationship between industry and academia that makes close cooperation between researchers and practitioners so important and monographs like this that combine both abstract concept and pragmatic implementation deftly bridge this often gaping chasm It was at the IEEE ACM Eighth International Symposium on Hardware Software Codesign where I met the author of this monograph Dr Randall Janka who was presenting some of his recent dissertation research results on specification and design methodology or as he has so succinctly defined this sometimes ambiguous concept the tools and rules Where so many codesign researchers are trying to prove out different aspects of codesign and using toy applications to do so Dr Janka had developed a complete specification and design methodology and prototyped the infrastructure and proven its viability utility and effectiveness using a demanding real world application of a real time synthetic aperture radar imaging processor that was implemented with embedded parallel processors *Multiprocessor Systems-on-Chips* Ahmed Jerraya,Wayne Wolf,2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs Design topics include multiprocessor architectures processors operating systems compilers methodologies and

synthesis algorithms and application areas covered include telecommunications and multimedia The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs After having refined their material at the workshop the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology Examines several different architectures and the constraints imposed on them Discusses scheduling real time operating systems and compilers Analyzes design trade off and decisions in telecommunications and multimedia applications **Architecture Design and Validation Methods** Egon Börger,2012-12-06 This book grew out of material which was taught at the International Summer School on Architecture Design and Validation Methods held June 23 July 5 1997 on the Island of Lipari and directed to graduate students and young researchers Since then the course notes have been completely elaborated and extended and additional chapters have been added so that this book offers a comprehensive presentation of the state of the art which leads the reader to the forefront of the current research in the area The chapters each of which was written by a group of eminent special ists in the field are self contained and can be read independently of each other They cover the wide range of theoretical and practical methods which currently used for the specification design validation and verification of are hardware software architectures Synthesis methods are the subject of the first three chapters The chapter on Modeling and Synthesis of Behavior Control and Data Flow focusses on techniques above the register transfer level The chapter on Cell Based Logic Optimizations concentrates on methods that interface logic design with phys ical design in particular on techniques for cell library binding the back end of logic synthesis The chapter on A Design Flow for Performance Planning presents new paradigms for iteration free synthesis where global wire plans for meeting timing constraints already appear at the conceptual design stage even before fixing the functionality of the blocks in the plan *Electronic Design Automation for IC System Design, Verification, and Testing* Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since

publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **EDA for IC System Design, Verification, and Testing** Louis Scheffer,Luciano Lavagno,Grant Martin,2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set **CASES ...** ,2005 **Computer Systems: Architectures, Modeling, and Simulation** Andy Pimentel,Stamatis Vassiliadis,2004-07-05 This book constitutes the refereed proceedings of the 4th International Workshop on Systems Architectures Modeling and Simulation SAMOS 2004 held in Samos Greece on July 2004 Besides the SAMOS 2004 proceedings the book also presents 19 revised papers from the predecessor workshop SAMOS 2003 The 55 revised full papers presented were carefully reviewed and selected for inclusion in the book The papers are organized in topical sections on reconfigurable computing architectures and implementation and systems modeling and simulation Design and Architecture for Signal and Image Processing Karol Desnos,Sergio Pertuz,2022-07-29 This book constitutes the thoroughly refereed conference proceedings of the First International Workshop on Design and Architecture for Signal and Image Processing DASIP 2022 held in Budaypest Hungary in June 2022 The 13 full included in the volume were carefully reviewed and selected from 32 submissions They are organized in the following topical sections leading signal image and video processing and machine learning in custom embedded edge and cloud computing architectures and systems

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