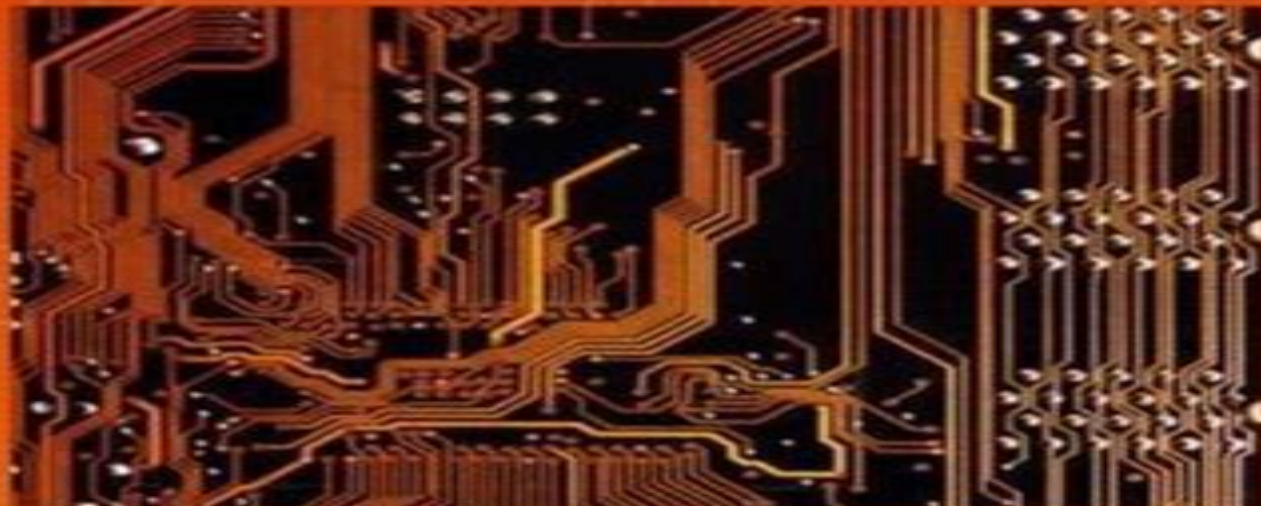


Symbolic Analysis and Reduction of VLSI Circuits

Chung-Kuan Cheng, Zhanhai Qin and Sheldon Tan



Symbolic Analysis And Reduction Of Vlsi Circuits

**Luis Miguel Silveira, Srinivas
Devadas, Ricardo A. Reis**



Symbolic Analysis And Reduction Of Vlsi Circuits:

Symbolic Analysis and Reduction of VLSI Circuits Zhanhai Qin, Chung-Kuan Cheng, 2009-03-13 Symbolic analysis is an intriguing topic in VLSI designs. The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation. However, analyzing circuits symbolically remains a challenging research issue. Therefore, in this book, we survey the recent results as the progress of on-going works rather than as the solution of the field. For parasitic reduction, we approximate a huge amount of electrical parameters into a simplified RLC network. This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time. A symbolic analysis approach reduces the circuit according to the network topology. Thus, the designer can maintain the meaning of the original network and perform the analysis hierarchically. For analog circuit designs, symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit. The analysis allows us to optimize the circuit behavior. The book is divided into three parts. Part I touches on the basics of circuit analysis in time domain and in s domain. For an s domain expression, the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform. On the other hand, the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain. Part II focuses on the techniques for parasitic reduction. In Chapter 2, we present the approximation methods to match the first few moments with reduced circuit orders. In Chapter 3, we apply the Y-Delta transformation to reduce the dynamic linear network. The method finds the exact values of the low-order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments. In Chapter 4, we handle two major issues of the Y-Delta transformation: common factors in fractional expressions and round-off errors. Chapter 5 explains the stability of the reduced expression; in particular, the Ruth-Hurwitz Criterion. We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks. In Chapter 6, we present techniques to synthesize circuits to approximate the reduced expressions after the transformation. In Part III, we discuss symbolic generation of the determinants and cofactors for the application to analog designs. In Chapter 7, we depict the classical topological analysis approach. In Chapter 8, we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation. In Chapter 9, we take only significant terms when we search through the determinant decision diagram to approximate the solution. In Chapter 10, we extend the determinant decision diagram to a hierarchical model. The construction of the modules through the hierarchy is similar to the Y-Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator. Therefore, we describe the method to prune the common factors. [Symbolic Analysis and Reduction of VLSI Circuits](#) Qin Zhanhai, Chung-Kuan Cheng, 2008-11-01 Symbolic analysis is an intriguing topic in VLSI designs. The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation. However, analyzing circuits symbolically remains a challenging research issue. Therefore, in this book, we survey the recent results as the progress

of on going works rather than as the solution of the field For parasitic reduction we approximate a huge amount of electrical parameters into a simplified RLC network This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time A symbolic analysis approach reduces the circuit according to the network topology Thus the designer can maintain the meaning of the original network and perform the analysis hierarchically For analog circuit designs symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit The analysis allows us to optimize the circuit behavior The book is divided into three parts Part I touches on the basics of circuit analysis in time domain and in s domain For an s domain expression the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform On the other hand the Taylor s expansion when s approaches zero derives the moments of the output responses in time domain Part II focuses on the techniques for parasitic reduction In Chapter 2 we present the approximation methods to match the first few moments with reduced circuit orders In Chapter 3 we apply the Y Delta transformation to reduce the dynamic linear network The method finds the exact values of the low order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments In Chapter 4 we handle two major issues of the Y Delta transformation common factors in fractional expressions and round off errors Chapter 5 explains the stability of the reduced expression in particular the Ruth Hurwitz Criterion We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks In Chapter 6 we present techniques to synthesize circuits to approximate the reduced expressions after the transformation In Part III we discuss symbolic generation of the determinants and cofactors for the application to analog designs In Chapter 7 we depict the classical topological analysis approach In Chapter 8 we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation In Chapter 9 we take only significant terms when we search through determinant decision diagram to approximate the solution In Chapter 10 we extend the determinant decision diagram to a hierarchical model The construction of the modules through the hierarchy is similar to the Y Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator Therefore we describe the method to prune the common factors

Advanced Symbolic Analysis for VLSI Systems Guoyong Shi, Sheldon X.-D. Tan, Esteban Tlelo Cuautle, 2014-06-19 This book provides comprehensive coverage of the recent advances in symbolic analysis techniques for design automation of nanometer VLSI systems The presentation is organized in parts of fundamentals basic implementation methods and applications for VLSI design Topics emphasized include statistical timing and crosstalk analysis statistical and parallel analysis performance bound analysis and behavioral modeling for analog integrated circuits Among the recent advances the Binary Decision Diagram BDD based approaches are studied in depth The BDD based hierarchical symbolic analysis approaches have essentially broken the analog circuit size barrier

Advanced Model Order Reduction Techniques in VLSI Design Sheldon Tan, Lei He, 2007-05-31 Model order reduction MOR techniques reduce the complexity of VLSI

designs paving the way to higher operating speeds and smaller feature sizes This book presents a systematic introduction to and treatment of the key MOR methods employed in general linear circuits using real world examples to illustrate the advantages and disadvantages of each algorithm Following a review of traditional projection based techniques coverage progresses to more advanced MOR methods for VLSI design including HMOR passive truncated balanced realization TBR methods efficient inductance modeling via the VPEC model and structure preserving MOR techniques Where possible numerical methods are approached from the CAD engineer s perspective avoiding complex mathematics and allowing the reader to take on real design problems and develop more effective tools With practical examples and over 100 illustrations this book is suitable for researchers and graduate students of electrical and computer engineering as well as practitioners working in the VLSI design industry Advances in Analog Circuits Esteban Tlelo-Cuautle,2011-02-02 This book highlights key design issues and challenges to guarantee the development of successful applications of analog circuits Researchers around the world share acquired experience and insights to develop advances in analog circuit design modeling and simulation The key contributions of the sixteen chapters focus on recent advances in analog circuits to accomplish academic or industrial target specifications **Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs** Ruijing Shen,Sheldon X.-D. Tan,Hao Yu,2014-07-08 Since process variation and chip performance uncertainties have become more pronounced as technologies scale down into the nanometer regime accurate and efficient modeling or characterization of variations from the device to the architecture level have become imperative for the successful design of VLSI chips This book provides readers with tools for variation aware design methodologies and computer aided design CAD of VLSI systems in the presence of process variations at the nanometer scale It presents the latest developments for modeling and analysis with a focus on statistical interconnect modeling statistical parasitic extractions statistical full chip leakage and dynamic power analysis considering spatial correlations statistical analysis and modeling for large global interconnects and analog mixed signal circuits Provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of VLSI systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits Helps chip designers understand the potential and limitations of their design tools improving their design productivity Presents analysis of each algorithm with practical applications in the context of real circuit design Includes numerical examples for the quantitative analysis and evaluation of algorithms presented Provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of VLSI systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits Helps chip designers understand the potential and limitations of their design tools improving their design productivity Presents analysis of each algorithm with practical applications in the context of real circuit design Includes numerical examples for the quantitative analysis and evaluation of algorithms presented VLSI: Systems on a Chip Luis Miguel Silveira,Srinivas Devadas,Ricardo A.

Reis,2013-11-11 For over three decades now silicon capacity has steadily been doubling every year and a half with equally staggering improvements continuously being observed in operating speeds This increase in capacity has allowed for more complex systems to be built on a single silicon chip Coupled with this functionality increase speed improvements have fueled tremendous advancements in computing and have enabled new multi media applications Such trends aimed at integrating higher levels of circuit functionality are tightly related to an emphasis on compactness in consumer electronic products and a widespread growth and interest in wireless communications and products These trends are expected to persist for some time as technology and design methodologies continue to evolve and the era of Systems on a Chip has definitely come of age While technology improvements and spiraling silicon capacity allow designers to pack more functions onto a single piece of silicon they also highlight a pressing challenge for system designers to keep up with such amazing complexity To handle higher operating speeds and the constraints of portability and connectivity new circuit techniques have appeared Intensive research and progress in EDA tools design methodologies and techniques is required to empower designers with the ability to make efficient use of the potential offered by this increasing silicon capacity and complexity and to enable them to design test verify and build such systems **Computer-Aided Design of Analog Integrated Circuits and Systems** Rob A.

Rutenbar,Georges G. E. Gielen,2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck *Advanced VLSI Design and Testability Issues* Suman Lata Tripathi,Sobhit Saxena,Sushanta Kumar Mohapatra,2020-08-18 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in

this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC s structure and function which makes it much more difficult to reverse engineer

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web place the frog in the dissecting pan ventral side up use scissors to lift the abdominal muscles away from the body cavity cut along the midline of the body to the forelimbs make transverse horizontal cuts near the arms and legs life the flaps of the body wall and pin back if your specimen is a female the body may be filled with eggs