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Smart Power ICs Bruno Murari, 2002-06-13 This book provides a survey of the state of the art of technology and future trends in the new family of Smart Power ICs and describes design and applications in a variety of fields ranging from automotive to telecommunications reliability evaluation and qualification procedures The book is a valuable source of information and reference for both power IC design specialists and to all those concerned with applications the development of digital circuits and with system architecture **Smart Power ICs** Bruno Murari, Franco Bertotti, Guioanni A.

Vignola, 2002-06-27 This survey of the state of the art of technology and future trends in the new family of Smart Power ICs describes design and applications in a variety of fields ranging from automotive to telecommunications reliability evaluation and qualification procedures Parasitic Substrate Coupling in High Voltage Integrated Circuits Pietro Buccella, Camillo

Stefanucci, Maher Kayal, Jean-Michel Sallese, 2018-03-14 This book introduces a new approach to model and predict substrate parasitic failures in integrated circuits with standard circuit design tools The injection of majority and minority carriers in the substrate is a recurring problem in smart power ICs containing high voltage high current switching devices besides sensitive control protection and signal processing circuits The injection of parasitic charges leads to the activation of substrate bipolar transistors This book explores how these events can be evaluated for a wide range of circuit topologies To this purpose new generalized devices implemented in Verilog A are used to model the substrate with standard circuit simulators This approach was able to predict for the first time the activation of a latch up in real circuits through post layout SPICE simulation analysis Discusses substrate modeling and circuit level simulation of parasitic bipolar device coupling effects in integrated circuits Includes circuit back annotation of the parasitic lateral n p n and vertical p n p bipolar transistors in the substrate Uses Spice for simulation and characterization of parasitic bipolar transistors latch up of the parasitic p n p n structure and electrostatic discharge ESD protection devices Offers design guidelines to reduce couplings by adding specific protections

Proceedings of the Symposium on High Voltage and Smart Power ICs Muhammed Ayman Shibib, 1989

Advances in Solid State Circuit Technologies Paul Chu, 2010-04-01 This book brings together contributions from experts in the fields to describe the current status of important topics in solid state circuit technologies It consists of 20 chapters which are grouped under the following categories general information circuits and devices materials and characterization techniques These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions Readers will be able to familiarize themselves with the latest technologies in the various fields **Lateral Power Transistors in Integrated Circuits** Tobias

Erlbacher, 2014-10-08 The book summarizes and compares recent advancements in the development of novel lateral power transistors LDMOS devices for integrated circuits in power electronic applications In its first part the book motivates the

necessity for lateral power transistors by a top down approach First it presents typical energy conversion applications in modern industrial automotive and consumer electronics Next it introduces common circuit topologies suitable for these applications and discusses the feasibility for monolithic integration Finally the combination of power and logic functionality on a single chip is motivated and the requirements and limitations for the power semiconductor devices are deduced The second part describes the evolution of lateral power transistors over the past decades from the simple pin type concept to double acting RESURF topologies It describes the principle of operation for these LDMOS devices and discusses limitations of lateral power devices Moreover figures of merit are presented which can be used to evaluate the performance of the novel lateral power transistors described in this book with respect to the LDMOS devices In the last part the fundamental physical concepts including charge compensation and trench gate topologies are discussed Also the status of research in LDMOS devices on silicon carbide is presented Advantages and drawbacks for each of these integration approaches are summarized and the feasibility with respect to power electronic applications is evaluated

Analog Circuit Design

Johan Huijsing, Michiel Steyaert, Arthur H.M. van Roermund, 2013-03-20 Analog Circuit Design contains the contribution of 18 experts from the 13th International Workshop on Advances in Analog Circuit Design It is number 13 in the successful series of Analog Circuit Design It provides 18 excellent overviews of analog circuit design in Sensor and Actuator Interfaces Integrated High Voltage Electronics and Power Management and Low Power and High Resolution ADC s Analog Circuit Design is an essential reference source for analog circuits designers and researchers wishing to keep abreast with the latest developments in the field The tutorial coverage also makes it suitable for use in an advanced design course

ESD

Protection Device and Circuit Design for Advanced CMOS Technologies Oleg Semenov, Hossein Sarbishaei, Manoj Sachdev, 2008-04-26 ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design VLSI reliability and testing domains As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry the demand for graduates with a basic knowledge of ESD is also increasing Today there is a significant demand to educate the circuits design and reliability teams on ESD issues This book makes an attempt to address the ESD design and implementation in a systematic manner A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance This methodology described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths

Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies

Stephan Henzler, 2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and

threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side *Guide to State-of-the-Art Electron Devices* Joachim N. Burghartz, 2013-03-19 Winner 2013 PROSE Award Engineering and Technology Concise high quality and comparative overview of state of the art electron device development manufacturing technologies and applications *Guide to State of the Art Electron Devices* marks the 60th anniversary of the IRE electron devices committee and the 35th anniversary of the IEEE Electron Devices Society as such it defines the state of the art of electron devices as well as future directions across the entire field Spans full range of electron device types such as photovoltaic devices semiconductor manufacturing and VLSI technology and circuits covered by IEEE Electron and Devices Society Contributed by internationally respected members of the electron devices community A timely desk reference with fully integrated colour and a unique lay out with sidebars to highlight the key terms Discusses the historical developments and speculates on future trends to give a more rounded picture of the topics covered A valuable resource R engineers in the semiconductor industry applied scientists circuit designers Masters students in power electronics and members of the IEEE Electron Device Society **Proceedings for the Second Workshop on Smart Power/Power Integrated Circuits: Technology and Applications**, 1994

Silicon Optoelectronic Integrated Circuits Horst Zimmermann, 2013-03-09 Explains the circuit design of silicon optoelectronic integrated circuits OEICs which are central to advances in wireless and wired telecommunications The essential features of optical absorption are summarized as is the device physics of photodetectors and their integration in modern bipolar CMOS and BiCMOS technologies This information provides the basis for understanding the underlying mechanisms of the OEICs described in the main part of the book In order to cover the topic comprehensively *Silicon Optoelectronic Integrated Circuits* presents detailed descriptions of many OEICs for a wide variety of applications from various optical sensors smart sensors 3D cameras and optical storage systems DVD to fiber receivers in deep sub m CMOS Numerous detailed illustrations help to elucidate the material **Operational Amplifier Speed and Accuracy Improvement** Vadim V. Ivanov, Igor M. Filanovsky, 2005-12-30 *Operational Amplifier Speed and Accuracy Improvement* proposes a new methodology for the design of analog integrated circuits The usefulness of this methodology is demonstrated

through the design of an operational amplifier This methodology consists of the following iterative steps description of the circuit functionality at a high level of abstraction using signal flow graphs equivalent transformations and modifications of the graph to the form where all important parameters are controlled by dedicated feedback loops and implementation of the structure using a library of elementary cells Operational Amplifier Speed and Accuracy Improvement shows how to choose structures and design circuits which improve an operational amplifier's important parameters such as speed to power ratio open loop gain common mode voltage rejection ratio and power supply rejection ratio The same approach is used to design clamps and limiting circuits which improve the performance of the amplifier outside of its linear operating region such as slew rate enhancement output short circuit current limitation and input overload recovery

The ESD Handbook Steven H. Voldman, 2021-03-02 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems

Analog Circuit Design Herman Casier, Michiel Steyaert, Arthur H.M. van Roermund, 2008-03-19 Analog Circuit Design is based on the yearly Advances in Analog Circuit Design workshop The aim of the workshop is to bring together designers of advanced analogue and RF circuits for the purpose of studying and discussing new possibilities and future developments in this field Selected topics for AACD 2007 are

- 1 Sensors Actuators and Power Drivers for the Automotive and Industrial Environment Tue 27 March Chaired by Herman Casier AMI Semiconductor Fellow Belgium
- 2 Integrated PA's from Wireline to RF Wed 28 March Chaired by Prof Michiel Steyaert Catholic University Leuven
- 3 Very High Frequency Front Ends Thu 29 March Chaired by Prof Arthur van Roermund Eindhoven University of Technology

High Dielectric Constant Materials Howard Huff, David Gilmer, 2005-11-02 Issues relating to the high K gate dielectric are among the greatest challenges for the evolving International Technology Roadmap for Semiconductors ITRS More than just an historical overview this book will assess previous and present approaches related

to scaling the gate dielectric and their impact along with the creative directions and forthcoming challenges that will define the future of gate dielectric scaling technology Topics include an extensive review of Moore's Law the classical regime for SiO₂ gate dielectrics the transition to silicon oxynitride gate dielectrics the transition to high K gate dielectrics including the drive towards equivalent oxide thickness in the single digit nanometer regime and future directions and issues for ultimate technology generation scaling The vision wisdom and experience of the team of authors will make this book a timely relevant and interesting resource focusing on fundamentals of the 45 nm Technology Generation and beyond *Analog Circuit*

Design Michiel Steyaert, Johan Huijsing, Arthur H.M. van Roermund, 2002-01-31 This tenth volume concentrates on three topics scalable analogue circuits high speed D/A converters and RF power amplifiers Each topic is covered by six papers written by an expert on that particular topic **System-level Test and Validation of Hardware/Software Systems**

Matteo Sonza Reorda, Zebao Peng, Massimo Violante, 2006-03-30 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability ESD Steven H. Voldman, 2009-07-01 Electrostatic discharge ESD failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a failure analysis and case study approach It provides a clear insight into the physics of failure from a generalist perspective followed by investigation of failure mechanisms in specific technologies circuits and systems The book is unique in covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology Look inside for extensive coverage on failure analysis tools EOS and ESD failure sources and failure models of semiconductor technology and how to use failure analysis to design more robust semiconductor components and systems electro thermal models and technologies the state of the art technologies discussed include CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVC MOS RF CMOS smart power gallium arsenide GaAs gallium nitride GaN magneto resistive MR giant magneto resistors GMR tunneling magneto resistor TMR devices micro electro mechanical MEM systems and photo masks and reticles practical methods to use failure analysis for the understanding of ESD circuit operation temperature analysis power distribution ground rule development internal bus distribution current path analysis quality metrics connecting the

theoretical to the practical analysis the failure of each key element of a technology from passives active elements to the circuit sub system to package highlighted by case studies of the elements circuits and system on chip SOC in today s products ESD Failure Mechanisms and Models is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic era

Insulated Gate Bipolar Transistor IGBT Theory and Design Vinod Kumar Khanna,2004-03-22 A comprehensive and state of the art coverage of the design and fabrication of IGBT All in one resource Explains the fundamentals of MOS and bipolar physics Covers IGBT operation device and process design power modules and new IGBT structures

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